A Comparison of n-T SRAM Cell in Nanometre Regime

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ABSTRACT
Now a day's low power SRAMs have become a critical component of many VLSI chips. This has especially true for microprocessors, where the demanding on chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory. Simultaneously, power dissipation has been becoming an important factor to recognise due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated applications. In this paper we have compared 4T, 6T, 7T, 8T and 9T SRAM cell at 65nm and 45nm technology by using HSPICE simulator and analyse in terms Power consumption, delay and PDP with supply voltage of 1V at 100MHz frequency.

Keywords
SRAM, SNM, Power consumption, PDP.

1. INTRODUCTION
SRAM memories are most essential element of any digital circuit. To store one bit data in SRAM cell minimum six transistors (6T) are required. Dynamic random access memory (DRAM) circuit is very simple compare to SRAM cell. In basic DRAM cell minimum only one transistor and a capacitor is required to stored single bit. The main advantage of DRAM over SRAM is its structural simplicity i.e. SRAM required six transistor but DRAM contains one transistor and one capacitor only. The read operation in the DRAM cell is more difficult and complex than the write operation. In this, read involves discharge of the initially capacitor with charge. So after every read operation the capacitor need to be charged. Every bit stored in SRAM with six transistors. This chapter means introduction part of thesis consists of discussion of the motivation, about different type of memories and overview of the thesis. SRAM is an important part of register file to determine its overall performance of memories. But in Deep Submicron Tech (DSM) as the size of the transistor is scaling down in nanometer technology. The issue of leakage power is most common in SRAM cells which are designed for a low power application. As a result the power consumption in SRAM design becomes a most common issue. But in low power design the speed of circuits degraded. So to optimize low power circuit without compromising with speed becomes the major concern of modern very large scale integration (VLSI) design. Furthermore due to scaling the circuit designs also faces design challenges for the circuit design for low power. The scaling causes the reduction in threshold voltage. For low Vth and ultra-thin gate oxide leads to the leakage power consumption [1]. The stability of the cell during read, write mode is also affected [2]. The supply voltage scaling becomes most effective technique for power saving. The scaling of supply voltage reduces the power consumption of the circuit in good amount [3]. But due to scaling of supply voltage and device size of SRAMs it affects process variation parameters and threshold voltage together. This leads to reduction in Static Noise Margin (SNM) that degrades cell stability [9, 10]. The static noise margin is linearly dependent on the supply voltage. The supply voltage is scaled down to reduce power consumption the stability of SRAM cell is affected. Hence to get low power SRAM design while maintaining the cell stability becomes the main theme of SRAM designs in modern scenario. In this thesis the 11T and 13T SRAM cells have been proposed with bit interleaving capability with better performance. Other design of SRAM cells with bit interleaving capability are presented in [4-8] in past.

1.1. Why SRAM?
The SRAM Array required more area of chip, since six transistors is required to store single bit. The SRAM, static RAM is more preferred compare with DRAM due to its high speed of operation. SRAM need not to require the data refreshment periodically. In case of Dynamic Random Access Memory (DRAM) requires the data refreshment periodically since it has a transistor and a capacitor in its structure. The refreshment is required in DRAM for data to remain valid. All the conventional SRAM cell is shown in Figure.1.

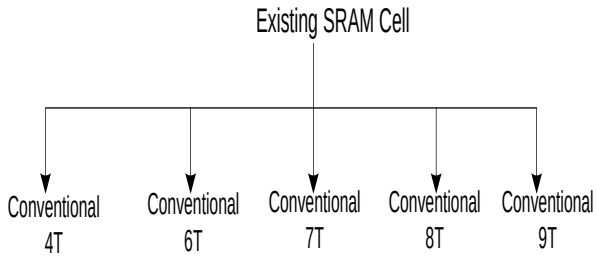

Figure.1 Flow diagram of Existing SRAM Cell

2. LITERATURE REVIEW
Now a day's to achieve better performances of SRAM cell, the devices are scaling down. The supply voltage and size of transistors are important parameters of any design. This causes the increment in sub threshold leakage current which leads to increase of static power dissipation. The Static power dissipation is mainly due to the sub threshold leakage current and gate leakage current. The RAM memory is volatile type of memory. That means data or information stored in the memory will be lost once the power supply switched off. Random access memory is used in computer for data storage. RAM memory is made up of integrated circuits which allow accessing of the stored data in random manner.

Anh-Tuan Do et. al [8] in this design An 8T differential SRAM has been proposed and have improved noise margin also have the bit-interleaving capability. The idea of the bit-interleaving is used first in this paper only later it used by others. The conventional 6T SRAM has the problem of stability degradation due to access disturbances at low power mode. Thus 8T and 10T cell design have been reported for improving the cell stability.

E. Seevinck et. al [10] in this paper the main work is on static noise margin for the stability analysis of the SRAM cell. The paper comprises more specifically stability analysis of SRAM of R load by static noise margin. Analytic expression for SNM of R load and full CMOS SRAM cell has been derived.

K. Takeda et. al [18] in this paper mainly work on the improvement of conventional 6T SRAM cell. The conventional 6T SRAM cell have problem during the read operation. This overcome by connecting an extra transistor which turns OFF during read operation. And also to help overcome limits to the speed of conventional SRAMs, a read-static-noise-margin-free SRAM cell have developed. To achieve the requirement some of transistor used with low threshold voltage. For the same speed this 7T have 23% smaller area than that of conventional SRAM.

3. STATIC RANDOM ACCESS MEMORY SRAM)

Write stability of SRAM cell can be analyzed by Write static Noise Margin (WSNM). The definition of the conventional WSNM based on the butterfly curve. The WSNM of circuit is equals to the smaller one of the two maximum squares in the butterfly curve i.e.

$$WSNM = \min (SNM\ 1, SNM\ 2)$$

Butterfly curves of standard 6T are shown in Figure.2. According to circuit we can get different shapes of curve and top side, bottom side may be different so, we can get different SNM then, we can count on the maximum SNM possible.

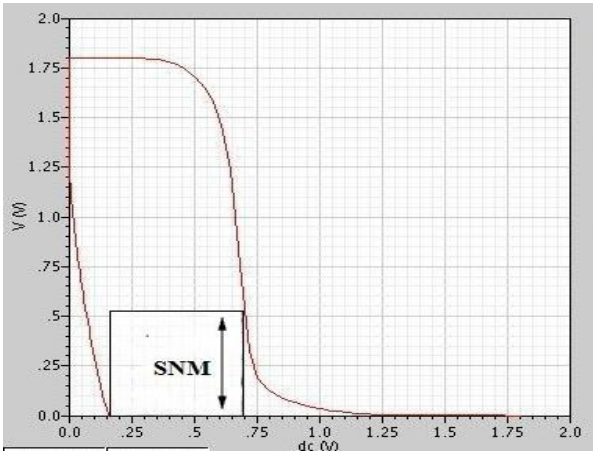

Figure.2. Statistical butterfly curves of 6T SRAM [4]

3.1 Conventional 6T SRAM Cell

The Conventional 6T SRAM cell is a combination of six transistors in which four transistors (M1 M2, M3 M4) are form two inverters. These two inverters are joined back to back in cross coupled manner. Apart from this two access NMOS transistors M5 and M6 acting as pass transistors and two data storing nodes (Q and QB). These data storing nodes are read by the pass or access transistor M5 and M6 as shown in Figure.2. These cross-coupled inverters forming the latch, i.e. each bit is stored in this cross coupled latch. These cross coupled inverters called data storing cell. The pass transistors M5 and M6 are used to access the data storing cell. The Word Line (WL) is used to enable these pass transistor M5 and M6 as shown in Figure.3. When the Word Line (WL) goes low, the pass transistors M5 and M6 are „OFF" and cell works in hold state or stand-by mode. This time reading of data or writing of data cannot be implemented, at this state latch will hold the bits for a long time. When the word line (WL) goes high.

3.1.1 Construction

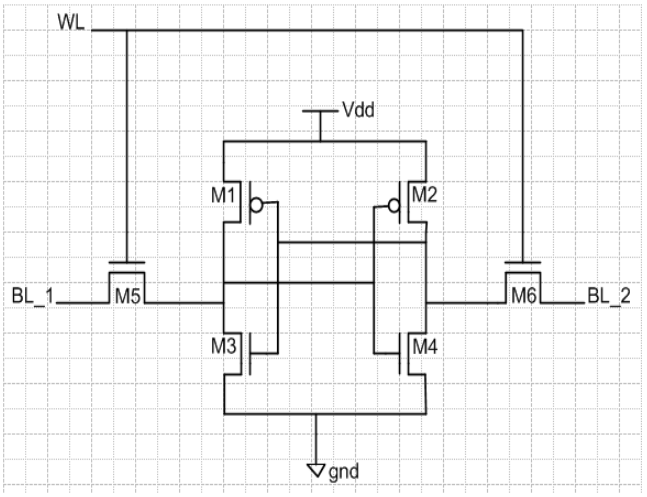

Figure.3. Conventional 6T SRAM cell [5]

For array construction in 6T SRAM cell shared word-line architecture is used. Even though share word line technique is simple and commonly used to arrange array of cell. The main drawback of this architecture is the multi-bit soft error is more severe. Since the adjacent bit share a WL each other.

3.1.2 Operation of SRAM

The Static Random Access memory device can perform the operation which is as follows: hold, read and write.

3.1.2.1 Hold

The cross-coupled inverters or data storing cell will continue with same data at both the data storing nodes. In this mode the current drawn from supply voltage is known as standby or leakage current. The power dissipation by this current is known to be standby power dissipation or leakage power dissipation.

3.1.2.2. READ

In read mode first set the word line WL to pre-charge to high voltage which turns on the pass transistors M5 and M6, when both the transistors turn on than the values of the output node Q and QB are transferred to bit line (BL) and BL bar (BLB) bit lines respectively but before giving the WL high the bit lines BL and BLB should be pre-charged to high voltage.

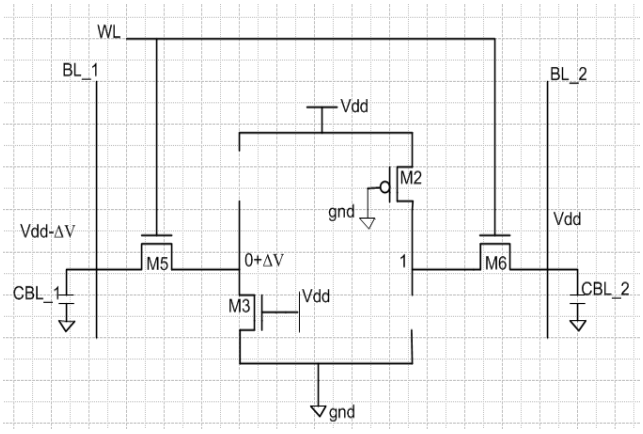

Figure.4. Read Operation of SRAM Cell [6]

The bit lines are pre-charged to VDD prior to initiating a read operation. The read operation is started by empowering the word line (WL) and connecting the pre-charged bit lines (BL_1 and BL_2) to the internal nodes of the cell. On read access, the bit line voltage VBL remains at the pre-charge level as shown in Figure.4. The complementary bit line voltage VBLB is discharged through transistors M1 and M5 connected in series. Conclusively, transistors M1 and M5 form a voltage divider whose output is now no longer at zero volts and is connected to the input of inverter M2−M4 (as in Figure 3.7.1). The sizing of M1 and M5 should ensure that inverter M2−M4 do not switch causing a destructive read [7-8].

3.1.2.3 Write:

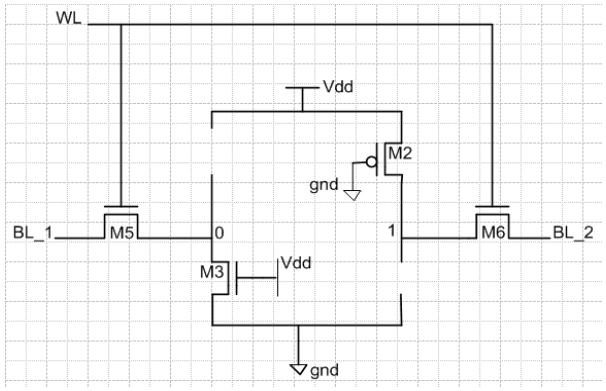

Figure .5. Write Operation of SRAM Cell [7]

In write operation, SRAM cell can write different bit value replacing its originally stored bit stored in the cell. To perform write operation, the access transistors (M5 and M6) are enabled using word line (WL =1) as shown in Figure.5. The required data to be written is given to bit line (BL), and its opposite data is given to bit line bar (BLB). That means for writing „1" in SRAM cell for this put the bit line at high voltage & bit line bar low (BLB=0) i.e. data write „1" at Q & opposite data write at QB thus the required data is written to the cell. [8].

3.2 7T SRAM

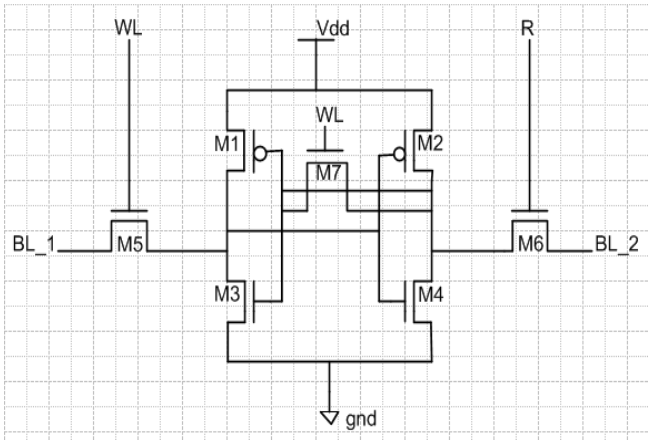

Figure .6. 7T SRAM cell [8]

The circuit of 7T SRAM cell is made of two CMOS inverters that are connected cross coupled to each other with additional NMOS Transistor which is connected to read line and has two pass NMOS transistors connected to bit lines and bit line bar respectively. Figure.6. shows circuit of 7T SRAM Cell, where the access transistors M5 is connected to the word-line (WL) to perform the access write and M6 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL_1 and BL_2). The bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation or from write in the memory cells during write operations [10-12].

3.3 8T SRAM Cell

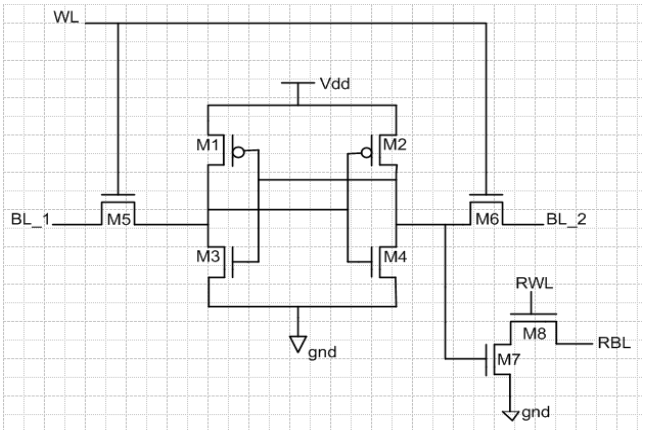

Figure.7. 8T SRAM cell [10]

The 8T SRAM circuit is presented in this section. The schematic of the 8T SRAM cell sized for a 65nm CMOS technology is shown in Figure.7. The left sub-circuit of the 8T memory cell is a conventional 6T SRAM cell with minimum sized devices (composed of M1, M2, M3, M4, M5, and M6). Two data access transistors (M5 and M6) and two bit lines (BL_1 and BL_2) are used for writing to the SRAM cell. An alternative communication channel (composed of a separate read bit line RBL and the transistor stack formed by M7 and M8) is used for reading the data from the cell [13].

3.4 9T SRAM cell

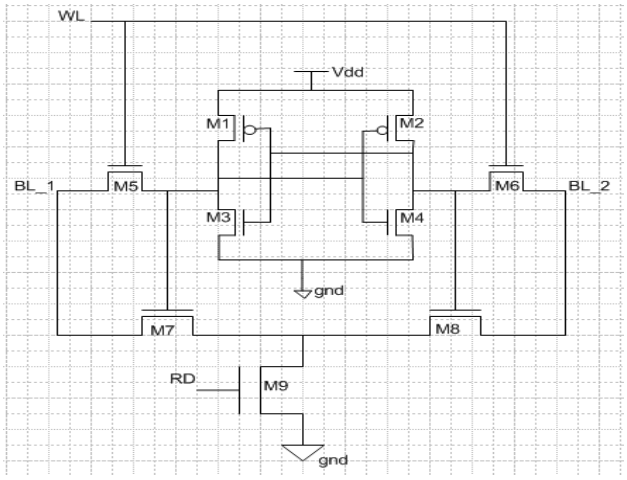

Figure.8. 9T SRAM cell [11]

The 9T SRAM consist of three extra transistors M7, M8, M9 compared to 6T SRAM cell. Transistor M7 is connected between node Q and M1 for the data protection for the duration of read operation [8]. The main motive of M5 transistor to prevent the discharging of node Q since it turns „OFF" during read operation. Transistor (M8, M9) forms a special inverter for AND logic operation [8] to trigger local word line (LWL). The 9T SRAM cell also has bit line (BL) for write operation, world line (WL) to activate LWL. For the read operation provide extra word line read word line (RWL).

The purpose of column bit line bar (CBLB) to control transistor M7

4. RESULTS AND DISCUSSION

In this table the results of 9T, 8T, 7T, 6T and Improved 4T SRAM cells are compared at the basis of parameters Power consumption, Delay and Static Noise Margin. In Table1, The proposed improved 4T SRAM cell shows maximum reduction in power consumption of 24.17% with 6T, of 88.6% with 7T, of 28.21% with 8T and of 35.03% with 9T, maximum reduction in delay of 9.1% with 6T, of 64.26% with 7T, of 9.18% with 8T and of 10.44%.

Table.I. Average Power and Delay of Conventional SRAMs Cells

SRAMS	Average Power Consumption(µW)		Delay (pS)			
			65nm		45nm	
	65nm	45nm	Max	Min	Max	Min
4T	0.144	0.233	19.37	7.859	15.35	9.670
6T	13.26	22.35	8.088	7.747	6.629	4.559
7T	16.71	30.19	7.357	2.753	1.502	0.631
8T	18.61	21.13	10.49	8.558	3.134	1.468
9T	24.55	38.12	8.595	8.008	6.000	3.741

The stability of SRAM cell is defined by static noise margin (SNM); the higher the SNM the better the stability. SNM of the SRAM cell is defined as the maximum DC noise voltage that a SRAM cell can survive without showing significant disturbances in the output bit or stored bit. So the cell stability varies with supply voltage. As supply voltage decreases, instability in the cell increases. The most common approach for measuring the SNM is by using butterfly curves, which is obtain from a dc simulation analysis as shown in Figure.9 and 6T SRAM provides proper logic as shown in Figure.10.

Table .II. PDP of Conventional SRAMs Cells

SRAMS	PDP (aJ)			
	65nm		45nm	
	Max	Min	Max	Min
4T	2.7922	1.1324	3.581	2.255
6T	107.31	102.79	148.2	101.8
7T	122.81	45.974	45.36	19.05
8T	40.519	33.050	19.22	9.005
9T	211.03	196.62	228.7	142.64

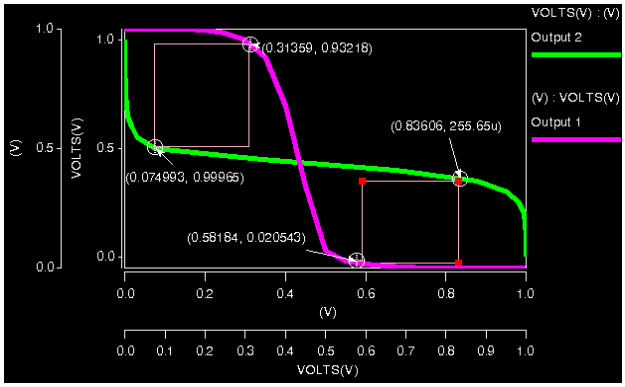

Figure.9. SNM curve of 6T SRAM cell

Figure.10. Output Waveform of Conventional 6T SRAM Cell

5. CONCLUSION

In this paper we have simulated and analyzed the performance of various topologies of SRAM cells at 65nm and 45nm technology for parameters like cell power consumption, delay and SNM. By comparative analysis of various topologies of SRAM cells; we can suggest that which SRAM cell topology is batter based on various analyzed parameters. The comparative results are given in Table 1 which shows that the power consumption, delay and SNM are minimum for 4T, 9T and 4T SRAM Cells and Maximum for 9T, 8T, and 6T SRAM Cells respectively. The results can be used to select SRAM cell topology to design and fabricate memory chips which is best suitable for different type of application.

6. REFERENCES

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