Abstract

The paper introduces designing of MAC 20 tap IIR filter based on Field Programmable Gate Array (FPGA). The implementation is based on Multiply Add and Accumulate algorithm (MAC) unit which plays important role in many of the DSP applications. MAC unit is used for best performance digital signal processing system. The designed filter has been synthesized on Digital Signal Processor (DSP) slice based FPGA to perform multiplier function of MAC unit. The proposed filter is implemented on two FPGA devices Xilinx’s Spartan-3E, xc3s500e-4fg320 and Vertex 2P, xc2vp30-5ff896 and compared on the basis of Direct-form I IIR and Direct-Form II IIR structure for hardware resource utilization as well as speed. The hardware result shows that the proposed low pass butterworth filter designed on spartan3E with Direct I Form 19.03% faster than that designed on vertex2p with Direct form II structure.

References

1. Rajesh Mehra, Bharti Thakur, “Field Programmable Gate Array Based Infinite Impulse
20 Tap Reconfigurable IIR Filter using Fully Parallel MAC Algorithm


Index Terms

Computer Science

Algorithms

Keywords

IIR low pass Butterworth filter, Matlab, Xilinx, FPGA, Spatan3E, Virtex2P