FPGA based Band Pass FIR Filter using Factored Canonic Signed Digit Technique for Satellite Application

Roshan Lal
ME Scholar (ECE)
NITTTR, Chandigarh, India

Rajesh Mehra, PhD
Associate Professor (ECE)
NITTTR, Chandigarh, India

Shallu
Research Scholar
NITTTR, Chandigarh, India

ABSTRACT
In this paper, an FPGA based FIR filter for Satellite Application is presented. The implementation is based on Factored Canonic signed digit (FCSD) which eliminates the use of embedded multipliers. The FIR filter has been implemented using Equiripple on an FPGA. In Equiripple, the ripples are distributed more evenly over pass band and stop band which results in a better approximation of desired frequency response can be achieved. The digital band pass filter used in satellite uplink model which is located before up converter. The uplink model used here is for C band small satellite communication system. With the performance evaluation of the equiripple filter design, it is found to be the most suitable and optimized method to meet the desired specification uplink model. An 89 tap FIR filter has been designed and simulated using 16 bit input and output precision in MATLAB environment. The behavioral simulation of VHDL model has been performed using ISE simulator. The simulated model has been synthesized using Xilinx synthesis tool (XST) on SPARTAN 3E based 3s500efg320-4 and Virtex 2P based 2vp30ff1152-5 target FPGA devices. The results depicts that FIR filter on Virtex 2P is 22.46% faster the SPARTAN 3E

General Terms
VHDL, CSD, Satellite Communication

Keywords
FCSD, FIR, uplink, FPGA, MATLAB

1. INTRODUCTION
Now a days digital signal processing is widely used in many applications like image processing, communication systems, bio-medical, multimedia etc. Digital filters play a vital role in all signal processing applications. Digital filters have numerous advantages over analog filters as these filters do not require precise value of input signal for their operation. These are also less sensitive to component tolerance and environmental changes. In digital signal processing, a single processor can be shared by multiple inputs by time sharing [1]. This decreases the processing cost. In addition to this, multi rate processing is possible only in digital domain. The main operation of digital filter design is coefficient calculation for transfer function to obtain response of that filter. Depending upon application it may be low pass, band pass or high pass filter. Digital filter are broadly classified into two categorized as finite impulse response (FIR) and infinite impulse response (IIR) [1].

Many DSP applications require a large order FIR filter. However, the computation complexity increases with increase in filter order because of requirement of larger computations .This poses a serious challenge in real time implementation of the filter with precise value. To achieve computationally efficient digital filter, order of FIR filter must be as low as possible. FIR filters are mainly focused due to its inherent stability and excellent linear phase characteristics. With respect to hardware implementation, digital filter can be categorized into two categories:

(i) Multipliers based

(ii) Memory based

Multipliers based design includes multiple constant multiplications (MCM) with add and shift operations [8]. MCM based FIR filter uses transposed form of structure which increases the speed of the system. The area can be further saved by optimizing coefficient with quantization technique. Memory based design are further categorized into two approaches: distributed arithmetic (DA) and Look Up table (LUTs) method. The distributed arithmetic approach calculates the inner product by accumulating bit level partial results in the FIR filter. The LUT based approach stores odd multiple of input signal in ROM to realize constant multiplications in MCM [2]. In order to reduce complexity, the FCSD representation is used for filter coefficients which require fewer adders [6].

The rest of the paper is organized as follows: an overview of Satellite uplink model, FIR filter and CSD and FCSD representation in section two. Section three consists of MATLAB simulated results based on filter specifications. Section four deals with hardware implementation. Finally, section five concludes the paper by summarizing the main contributes. Section six includes references.

2. SATELLITE UPLINK MODEL
Microwave C band has many desirable features such as less propagation problem, low rain attenuation, sky noise that resists snow effects and might have a maximum output power. The standard C band for satellite uplink is 5.925 to 6.425 GHz [3]. The satellite uplink system used in this paper is shown in Fig.1. It has five main blocks such as Encoder, IF Modulator, Band pass filter, Up-converter and High Power Amplifier [3]. The input baseband signal is applied to the encoder and passes through the modulator. The modulated output further goes to the digital band pass filter. The filtered output is up-converted and sent to the antenna system using high power amplifier. Finally, the antenna transmits the desired signal to the transponder of satellite.

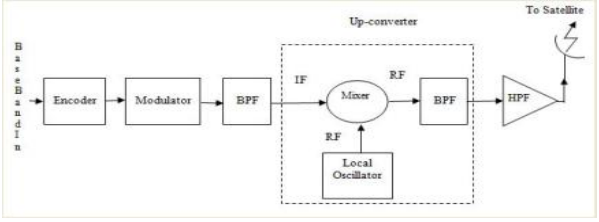

Figure 1.Satellite uplink model

The digital band pass filter is more suitable for small satellite uplink system to remove noise. The advantages of digital band pass filter are that it is convenient in designing, small in size and low insertion loss. The FIR equiripple digital filter is very useful and an efficient technique over other filter design for removing noise, spectrum shaping and reducing inter-symbol noise in satellite communication [3].The band pass filter is used after modulator and before up-convertor is a finite impulse response type filter.

2.1 The Fir Filter

The structure of FIR filter made up of multipliers, delay elements and adders to give the filter's output [4]. The recursive FIR filters can be represented as difference equation of N order

$$y\,(n) = \sum_{k=0}^{N-1} h\,(n)x(n-k) \qquad (1)$$

$$y\,(n) = \sum_{k=0}^{N-1} b_k\,x(n-k) \qquad (2)$$

Where, y (n) is the output sequence, h (n) is the impulse response and k is the order of the filter. The output signal is obtained by convolution of the input sequence x (n) and the impulse response h (n).

$$y(n) = x(n) * h(n) \qquad (3)$$

Or equivalently,

$$y(n) = x(0) * h(n) + x(1) * h(n-1) + \cdots x(n) * h(0) \qquad (4)$$

The system function H (z) can be expressed as using z-transform:

$$H\,(z) = \sum_{k=0}^{N-1} b_k z^{-k} \qquad (5)$$

Where the coefficient b_k equals to the successive value h (n).The system function H (z) is polynomial of z^{-1}. It means that all poles are only plotted at the origin of the z-plane [4]. Depending upon calculation of filter coefficients ,design of FIR filters can be can be done in various ways, for example window technique, weighted least squares method ,optimal equiripple method and frequency sampling technique. This paper focuses on design of FIR filter using equiripple method and realized using direct form as shown in figure 2.

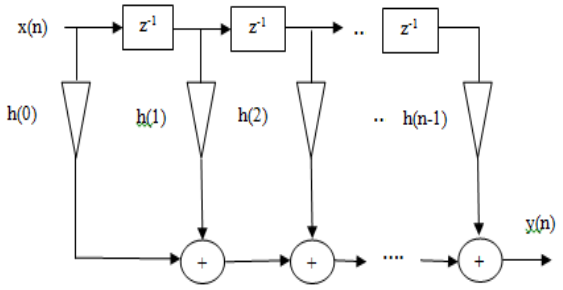

Figure 2.Direct form FIR Filter

The flow chart given below shows step by step procedure to design FIR filter.

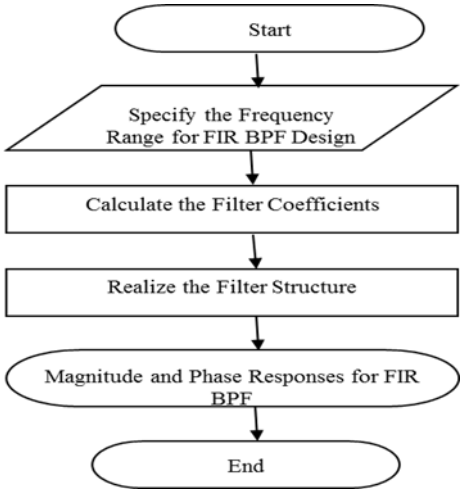

Figure 3.Flow chart for filter design

2.2 The CSD and FCSD Representation

There are two approaches to deal with computation of filter coefficients, the first approach is to represent the tap values in binary number, and another one is CSD (canonic signed digit) number representation. The canonical-signed-digit (CSD) is a number system for encoding a floating-point value in a two's complement representation. Results shows that this scheme contains approximately 33% fewer non-zeros than the two's complement form, leading to more efficient implementations of add/subtract operations in hardwired DSP processor [5]. The CSD representation is ternary number system uses symbols, -1, 0, +1 with each position representing the addition or subtraction of a power of 2. For example consider a number 99 which is represented as (+0–00+0–) in CSD. A digital filter structure will be canonic if the number of delays in the block diagram representation is equal to the order of the transfer function. The aim of this is to reduce the precision of coefficients and thus the filter complexity without affecting the filter performance. Encoding a binary number such that it contains the fewest number of non-zero bits is called canonic signed digit (CSD) .The following are the properties of CSD representation of a number [5]:

1. No two consecutive bits in a CSD representation are non-zero.
2. It contains the minimum possible number of non-zero bits
3. It is a unique number.

In canonical signed digit (CSD) or factored CSD techniques the multiplier operations are replaced by additions of partial products produced by CSD or factored CSD techniques. These techniques minimize the number of addition operations required for constant multiplication by representing binary numbers with a minimum count of nonzero digits [7].

Factored Canonical Signed Digit representation is a slight modification over CSD. In FCSD, the prime factorization of the coefficients is used. It replaces multiplier operation with add and shift operations. CSD representation of filter coefficients with effective factorization reduces the number of adders and filter area which in turn decreases hardware cost but all these benefits are achieved at the cost of decreased clock speed. Increase in propagation delay is the major drawback of this algorithm. The example given below compares CSD and FCSD technique:

y = 99*x

= (128– 32+4– 1) * x

= (+0–00+0–) *x % 99 in signed digit

= (x << 7) –(x << 5) + (x << 3) – x

Cost of CSD in terms of adders = 1addition and 2 subtraction operation.

y = 99*x

= (3*33)* x

= (x << 2– x) *(x << 5 + x)

Cost of FCSD in terms of adders = 1 addition and 1 subtraction operation.

It can be said that the number of adders has been reduced by using FCSD instead of CSD technique. Therefore, one can use FCSD formulation for reducing filter complexity [5, 6].

3. MATLAB BASED SILMULATON

The designing of FIR equiripple band pass filter for satellite uplink model requires the knowledge of parameter such as pass band frequency, pass band ripple, stop band attenuation, sampling frequency and transition frequency. The filter specifications implemented in MATLAB environment

Table 1.Filter Specifications

Filter parameters	Value
Design Method	Equiripple
Architecture	Partially serial
Sampling frequency, Fs	450 MHz
Pass band frequency, Fpass	70-140 MHz
Lower stop band frequency,fstop1	0-60 MHz
Upper stop band frequency,fstop2	150-210 MHz
Stop band attenuation	60dB
Pass band attenuation	1dB

On basis of these specifications, the filter order of 89 is obtained. The filter coefficients obtained from designing of filter are shown in table 2.

Table 2.Filter Coefficients

h0 = h89 = -0.00151	h23 = h66 = -0.0202
h1 = h88 = 0.00220	h24 = h65 = -0.0051
h2 = h87 = 0.00604	h25 = h64 = 0.0220
h3 = h86 = -0.00369	h26 = h63 = 0.0055
h4 = h85 = -0.01205	h27 = h62 = 0.0011
h5 = h84 = 0.00272	h28 = h61 = 0.0107
h6 = h83 = 0.01421	h29 = h60 = -0.0242
h7 = h82 = 0.00020	h30 = h59 = -0.0292
h8 = h81 = -0.00774	h31 = h58 = 0.0208
h9 = h80 = -0.00053	h32 = h57 = 0.0167
h10 = h79 = -0.00404	h33 = h56 = 0.0024
h11 = h78 = -0.00378	h34 = h55 = 0.0329
h12 = h77 = 0.01071	h35 = h54 = -0.0124
h13 = h76 = 0.00696	h36 = h53 = -0.0710
h14 = h75 = -0.00597	h37 = h52 = 0.0000
h15 = h74 = -0.00098	h38 = h51 = 0.0325
h16 = h73 = -0.00381	h39 = h50 = -0.0044
h17 = h72 = -0.01147	h40 = h49 = 0.0884
h18 = h71 = 0.00696	h41 = h48 = 0.0700
h19 = h70 = 0.01526	h42 = h47 = -0.2141
h20 = h69 = -0.00218	h43 = h46 = -0.1796
h21 = h68 = -0.00053	h44 = h45 = 0.2510
h22 = h67 = -0.00001	

These filter coefficients are symmetric hence this filter is stable and has linear phase response.

4. HARDWARE IMPLIMEMENTAION

In the recent years, there has been a growing trend to implement digital signal processing functions in Field Programmable Gate Array (FPGA) [10].The Xilinx Integrated Software Environment (ISE) 10.2 is used for implementation of design. The VHDL model is synthesized on SPARTAN 3sd1800acs484-5 and Virtex 5 based 5vlx50tff1136-3 target FPGA devices respectively [9].

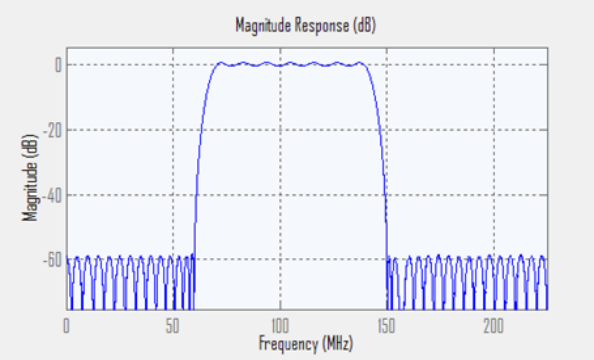

Figure 4.Magnitude Plot of Equiripple Band Pass Filter

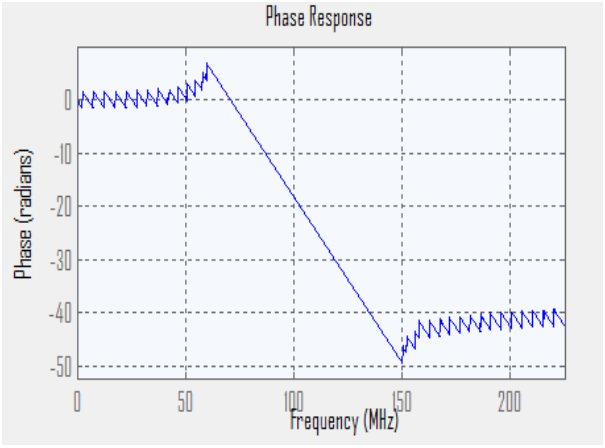

Figure 5.Phase Response

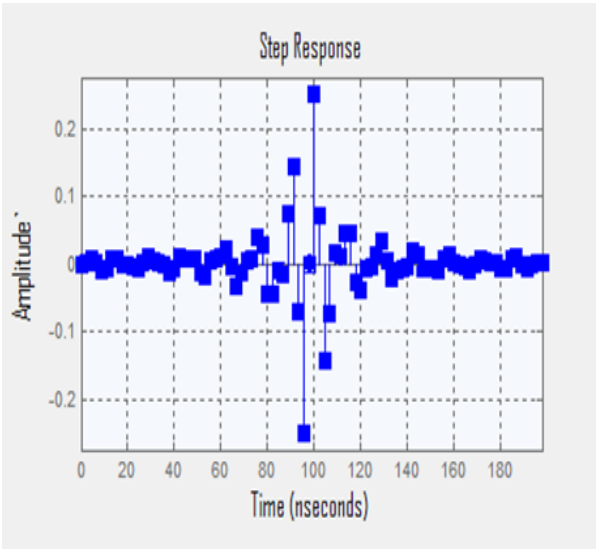

Figure 6.Step Response

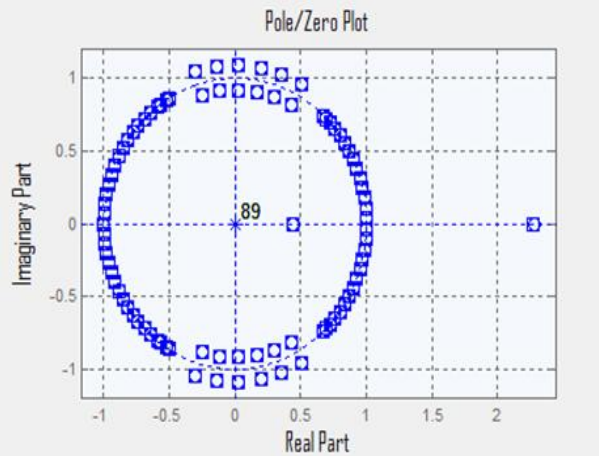

Figure 7.Pole Zero Plot

Table 3.Device Utilization of SPARTAN 3E

SPARTAN 3E		
Parameters	Used/Available	% Utilization
Number of Slices	1466 out of 4656	31%
E Number of 4 input LUTs	1293 out of 9312	13%
Number of bonded IOBs	35 out of 232	15%
Number of multipliers	4 out of 20	20%
Maximum Frequency	59.089MHz	

Table 4.Device Utilization of VIRTEX 2P

VIRTEX 2P		
Parameters	Used/Available	% Utilization
Number of Slices	1468 out of 13696	10%
Number of 4 input LUTs	1350 out of 27392	4%
Number of bonded IOBs	35 out of 644	5%
Number of multipliers	4 out of 136	2%
Maximum Frequency	72.365 MHz	

Table 5.Comparision for device utilization in SPARTAN 3E And VIRTEX 2P

Parameters	SPARTAN 3E	VIRTEX 2P
Number of Slices	31%	10%
Number of 4 input LUTs	13%	4%
Number of bonded IOBs	15%	5%

Table 6.Speed and Time Delay

Parameters	SPARTAN 3E	VIRTEX 2P
Maximum Frequency	59.089MHz	72.365 MHz

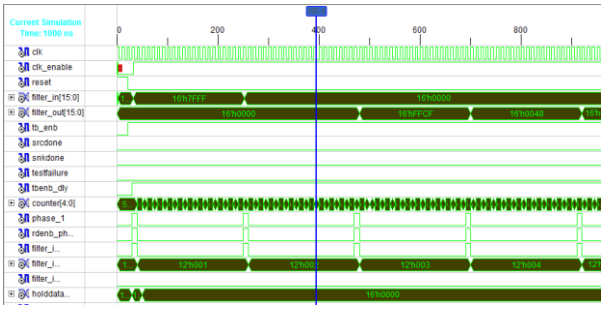

Figure 8 Simulation result on SPARTAN 3E

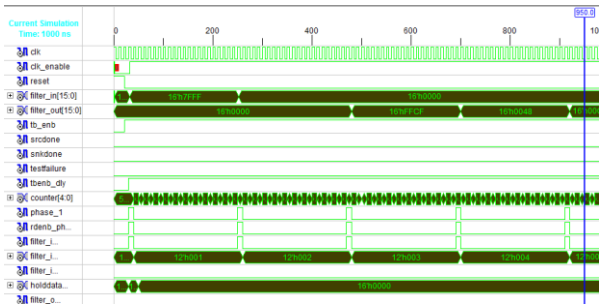

Figure 9. Simulation result on VIRTEX 2P

5. CONCLUSION

In this brief, a FPGA based band pass FIR filter using factored canonic signed digit technique for satellite application is proposed .In this paper the simulated VHDL model has been synthesized using Xilinx synthesis tool (XST) on SPARTAN 3s500efg320-4 and Virtex 2P based 2vp30ff1152-5 target FPGA devices. The results shows that Virtex 2Pis 22.46% more faster as compare to SPARTAN 3E.The SPARTAN 3E can be operated at a maximum delay of 16.92 ns by utilizing 1466 slices, and 1293 look up tables (LUTs) to provide Signal Processing where Virtex 2 can operated at a maximum delay of 13.81 ns by utilizing 1468 slices, and 1350 look up tables (LUTs) to provide Signal Processing. The later has better speed performance [5].Moreover it is concluded that Virtex 2P target FPGA device should be used because of lesser time delay.

6. REFERENCES

[1] Kumudini Sahu, Rahul Sinha, "FIR Filter Designing using MATLAB Simulink and Xilinx system Generator," International Research Journal of Engineering and Technology ISSN: 2277-3878, Volume: 02 Issue: 08 | Nov-2015, pp. 1608-1611.

[2] Neha Goel, Ashutosh Nandi,"Design of FIR Filter Using FCSD Representation," IEEE International Conference on Computational Intelligence & Communication Technology978-1-4799-6023-1/15 © 2015 IEEE,pp.617-620

[3] Aye Than Mon, Zaw Min Naing, Chaw Myat New, Hla Myo Tun, "Development Of Digital Band Pass Filter And Antenna Design For C Band Small Satellite Uplink Model," International Journal Of Scientific &

Technology Research Volume 3, Issue 7, July 2014, pp. 216-222.

[4] Rohit Patel, Er. Mukesh Kumar, Prof. A.K. Jaiswal, Er. Rohini Saxena, "Design Technique of Bandpass FIR filter using Various Window Function," IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) ISSN: 2278-8735. Volume 6, Issue 6 (Jul. - Aug. 2013), pp 52-57

[5] Kanu Priya, Rajesh Mehra, "FPGA Based Cost Efficient Fir Filter Using Factored CSD Technique," International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-1, Issue-6, January 2013, pp. 130-133.

[6] Neha Goel, Ashutosh Nandi," Design of Optimized FIR Filter Using FCSD Representation" International Journal of Electrical & Electronics Engg. e-ISSN: 1694-2310 | p-ISSN: 1694-2426, Vol. 2, Spl. Issue 1 (2015)

[7] R. M. Hewlitt and E. S. Swartzlantler, Jr., "Canonical signed digit representation for FIR digital filters," in *Proc. IEEE Worksh. SignalProcess. Syst.*, 2000, pp. 416–426.

[8] Kuan-Hung Chen and Tzi-Dar Chiueh, "A Low-Power Digit-Based Reconfigurable FIR Filter,"IEEE Transactions On Circuits And Systems—Ii: Express Briefs, Vol. 53, No. 8, August 2006, pp. 130-133.

[9] Farzad Nekoei, Yousef S. Kavian, Otto Strobel, "Some Schemes Of Realization Digital FIR Filters On FPGA For Communication Applications," 20th Int. Crimean Conference"Microwave & Telecommunication", 13-17 September,Sevastopol pp. 616-619.

[10] Rajesh Mehra, Ravinder Kaur,"FPGA based Efficient Interpolator design using DALUT Algorithm," Nabendu Chaki et al. (Eds.): NeTCoM 2010,CSCP 01, pp. 51–62, 2011.

7. AUTHOR PROFILE

Roshan Lal: Mr. Roshan has received his B.E. degree in Electronics and Communication Engineering from Rajasthan University, Jaipur (Raj.) in 2006. Currently, he is pursuing his M.E from National Institute of Technical Teachers, Training & Research, Chandigarh, India. He is Lecturer at Government Polytechnic College, Barmer (Raj.) His research area includes Signals and Systems, Advanced Digital Signal Processing and VLSI Design.

Dr. Rajesh Mehra: Dr. Mehra is currently associated with Electronics and Communication Engineering Department of National Institute of Technical Teachers' Training & Research, Chandigarh, India since 1996. He has earned his Doctor of Philosophy in Engineering & Technology and Master of Engineering from Panjab University, Chandigarh, India. He has completed his Bachelor of Technology from NIT, Jalandhar, India. Dr. Mehra has 20 years of academic and research experience. He has more than 350 papers to his credit which are published in refereed International Journals and Conferences. Dr. Mehra has guided 80 ME thesis and he is also guiding 02 PhD scholars. He has also authored one book on PLC & SCADA and developed 06 video films in VLSI area. His research areas are Advanced Digital Signal Processing, VLSI Design, FPGA System Design, Embedded System Design, and Wireless & Mobile Communication. Dr. Mehra is member of IEEE and ISTE.