Abstract

In this paper, Asynchronous FIR filter is designed and implemented for ECG signal processing. The use of asynchronous design approaches to construct digital signal processing (DSP) systems is a rapidly growing research area driven by a wide range of emerging energy constrained applications such as wireless sensor network, portable medical devices and brain implants. This inherent advantage of asynchronous design over conventional synchronous circuits allows them to be energy efficient. The technique used for the design and implementation is modified pipelining representation. This paper describes the analyzing and modelling of asynchronous design FIR equiripple filter using MATLAB, simulated with ISE and then implemented on FPGA devices. The proposed Asynchronous design FIR equiripple filter is implemented on two FPGA devices Xilinx’s Spartan-3E, xc3s500e-4fg320 and Virtex 2P, 2vp30ff1152-5 and compared on the basis of Asynchronous FIR and Synchronous FIR filter for hardware resource utilization as well as speed. The hardware result shows that the proposed asynchronous designed on Virtex 2P is 10.72% faster than that designed on synchronous FIR filter on given specifications. The designed FIR filter on FPGA device Virtex 2P shows efficient
area utilization as well as better speed as compared to that designed with synchronous FIR filter.

References


12. AUTOR PROFILE

13. Rahul Sharma: Rahul Sharma is a M.E. scholar from National Institute of Technical Teachers Training and Research, Chandigarh India. He is having two years of teaching experience. He has completed his B.Tech from Green Hills Engineering college Solan (H.P.) from Himachal Pradesh University Shimla (H.P.) in June 2013. His interest Areas are Digital Signal Processing, Digital Communication, VLSI Design, wireless mobile Communication and Digital Electronics.

14. Dr. Rajesh Mehra: Dr. Mehra is currently associated with Electronics and Communication Engineering Department of National Institute of Technical Teachers’ Training & Research, Chandigarh, India since 1996. He has earned his Doctor of Philosophy in Engineering &Technology and Master of Engineering from Punjab University, Chandigarh, India. He has completed his Bachelor of Technology from NIT, Jalandhar, India. Dr. Mehra has 20 years of academic and research experience. He has more than 350 papers to his credit which are published in refereed International Journals and Conferences. Dr. Mehra has guided 80 ME
thesis and he is also guiding 02 PhD scholars. He has also authored one book on PLC & SCADA and developed 06 video films in VLSI area. His research areas are Advanced Digital Signal Processing, VLSI Design, FPGA System Design, Embedded System Design, and Wireless & Mobile Communication. Dr. Mehra is member of IEEE and ISTE.

15. Chandni received her B.E. degree in Electronics and Communication Engineering from the Himachal Pradesh University in 2010, and M.E. degree in ECE Engineering from Punjab University in 2013. In 2013, she joined the Department of Electronics and Communication Engineering of Baddi University, as an Assistant Professor. She was the Convener of the National Conference on Recent Innovations in Electronics, Electrical and Computer Engineering held in Baddi University, Himachal Pradesh. In December 2015 she enrolled for PhD. in National Institute of Technical Teacher’s Training & Research, Chandigarh. Her current research interests include VLSI Design, Digital Signal Processing, and Nano electronic Devices.

**Index Terms**

Computer Science  
Signal Processing

**Keywords**

Asynchronous FIR Filter, ECG, Filter, MATLAB, Xilinx.