Comparative Analysis of 4x4 Vedic and Conventional Multiplier with different Adders at 32 nm Technology

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ABSTRACT
Processor speed largely governed by the multiplier architectures. It is desired to have faster ALU with lower power consumption for portable applications to have good battery life. Hence, there is need to address different multiplier architectures. In this paper, the analysis of 4-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) and conventional multiplier with two different adders has been realized using carry look ahead adder and ripple carry adder. Comparative study of multipliers is done for low power requirement and high speed. The main purpose of the paper is to investigate the better adder and multiplication technique. It is observed that the conventional multiplier with CLA adder is more stable and power efficient. Conventional multiplier with CLA adder is having 117 % less energy delay product than Vedic with RCA adder, 62.0 % less than CLA based Vedic multiplier and 30.7 % less than conventional multiplier with RCA adder at supply voltage 0.9 V. Conventional multiplier with CLA adder is good over RCA adder based multiplier

Keywords
Energy Delay Product (EDP);Ripple Carry Adder; Carry look ahead adder; Energy Delay Product (EDP)

1. INTRODUCTION
Multiplication is the most important arithmetic operation in signal processing applications [1]. Vedic mathematics [2] was reconstructed from the ancient Indian scriptures (Vedas).Vedic mathematics is based on sixteen word-formulae which are known as sutras. As multipliers are the main component of many handheld devices, the power requirements are more stringent for them as shown in figure 1, Hence there is a requirement of efficient low power and low area multipliers. In 1980, the major concerns were high speed, less area and low cost, whereas power considerations are now playing very important role in portable devices [3]. This work presents a systematic design methodology for 4x4 Vedic multiplier based on Vedic mathematics and conventional multiplier [4]. Conventional CMOS design technique both logic-1 and logic-0 are transferred exactly at the output with same applied voltage level but at the expense of more area and high power consumption. In CMOS circuits, power dissipation primarily occurs during device switching. This

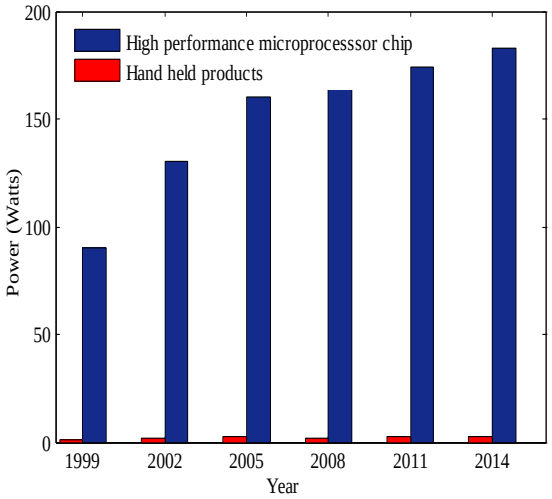

Fig 1: Power requirements of the microprocessor chip and portable products as per ITRS [5-6].

paper presents the CMOS technique for implementation of low power and high speed VLSI with metal gate bulk device and different topology style.

This paper presents the CMOS technique for implementation low power and high speed VLSI with metal gate bulk device and different topology style. The important matrix considerations for VLSI design are delay, power and area. There are many proposed logics (or) low power dissipation and high speed and each logic style have its own advantages in terms of speed and power [7-8].This paper presents a simple digital multiplier architecture [9] based on the ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra in with two adders one is ripple carry adder and another one is carry look ahead adder are used. In this paper, the performance parameters of delay, average power and Energy delay product are compared at different topology [10]. It is observed that the conventional multiplier with CLA adder is more stable and power efficient. This paper is organized as below. Section II introduces 4-bit ripple carry adder and Carry look ahead adder analysis for the delay. Section III elaborates multiplier details, Section IV shows simulation results and Section V draws the conclusion.

2. RCA AND CLA

2.1 RCA

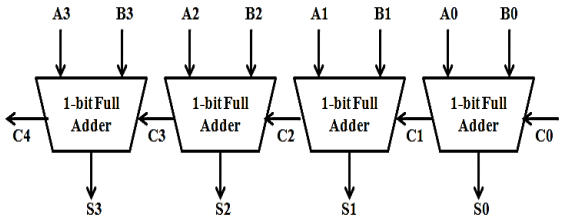

Fig 2: 4 bit RCA full adder

In a 4-bit ripple-carry adder shown in figure 2, there are 4 full adders, so the critical path [10] delay is equal to 3 for the first adder, 3 multiplied by 2 for a propagation of carry in later adder's gives total 9 gate delays. The equation for the critical path delay for carry-ripple adder n-bits is

$$T_{CRA}(n) = T_{HA} + (n-1) * T_C + T_S$$
$$= T_{FA} + (n-1) * T_C$$
$$= 6D + (n-1)2D$$
$$= (n+2)*2D$$

2.2 CLA

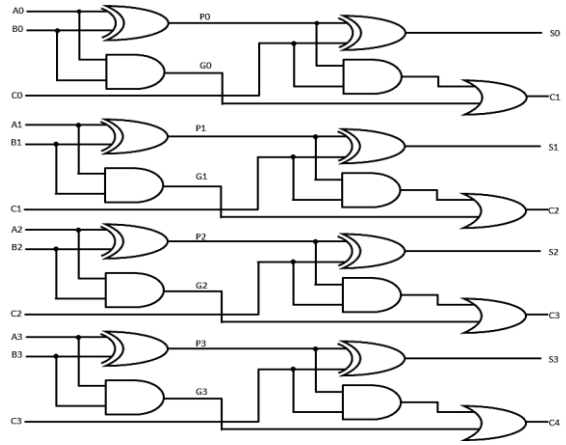

Fig 3: 4 bit CLA adder

The critical path of a full adder runs through both XOR-gates and ends at the sum bit S. Assumed that an XOR-gate takes 3 delays to complete. The delay imposed by the critical path of a full adder is equal to

$$T_{FA}=2*T_{XOR}=2*3D=6D$$

The carry-block subcomponent consists of 2 gates and therefore has a delay of

$$T_C=2D$$

the critical path of a full adder is given below.

$$C_1 = G_0 + P_0C_0$$

$$C_2 = G_1 + P_1C_1 = G_1 + P_1(G_0 + P_0C_0)$$
$$= G_1 + P_1G_0 + P_1P_0C_0$$

$$C_3 = G_2 + P_2C_2 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$$

$$C_4 = G_3 + P_3C_3$$
$$= G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

A 4 bit carry look ahead adder is shown in figure 2.

3. 4-BIT MULTIPLIER

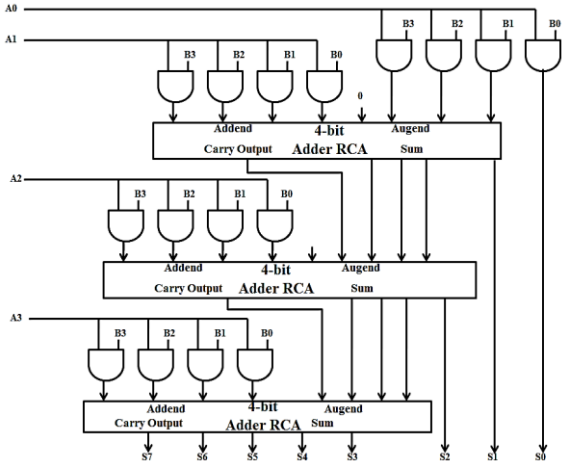

Fig 4: 4X4 Conventional multiplier

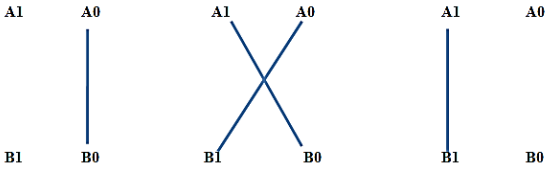

Fig 5: 2-bit Vedic multiplication

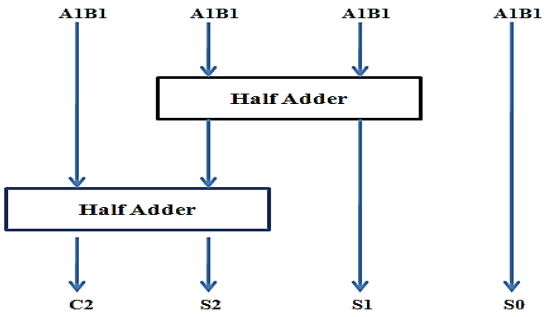

Fig 6: Block diagram of 2x2 bit Vedic multiplier

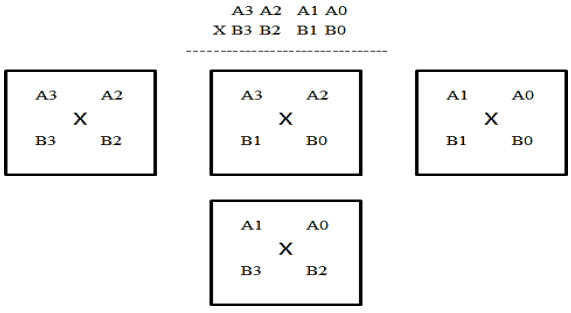

Fig 7: 4X4 Vedic multiplication

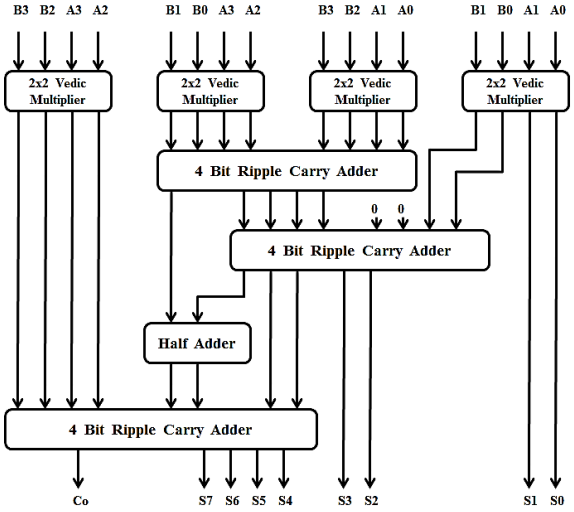

Fig 8: Block Diagram of 4-bit Urdhva multiplier with Ripple carry adder

CMOS technique is used to design adders and multiplier. Multipliers are designed using conventional technique and Vedic. A bulk device which is used is 32nm metal gate high k model from PTM library having supply voltage 0.9V and a threshold voltage of NMOS is 0.3558V and for PMOS threshold voltage is -0.24124V. All these parameters have been taken from predictive technology model. Different comparison of Average power, delay, and Energy product delay has compared for two different adders and multiplier in this paper. Figure4 shows conventional multiplier with RCA adder same is used replacing CLA adder[11-12].Figure 5 shows the 2-bit binary number multiplication, figure 6 shows 2x2 multiplier arrangement[13-15]. Figure 7 shows the 4X4 multiplication; same is implemented shown in figure 8 where RCA adder is replaced with CLA and both has been simulated in H-spice software. All the results have been compared in this section.

4. SIMULATION RESULTS

4.1 Conventional and Vedic Multiplier with Ripple carry adder

4.1.1 V_{DD} variations

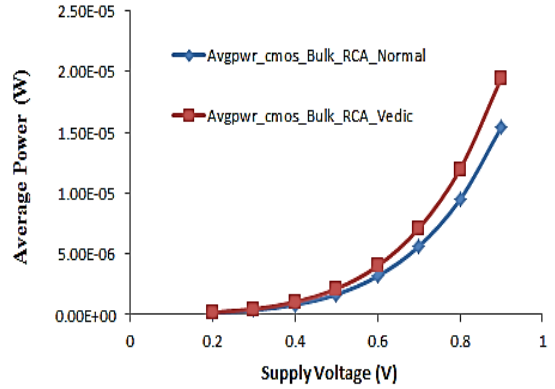

Fig 9: Average Power as function of supply voltage

Figure 9 shows the comparison of average power as the function of supply voltage for Vedic multiplier and conventional multiplier with RCA adder using the bulk device of 32nm. It is observed that the conventional multiplier is having less power than the Vedic multiplier.conventional multiplier with RCA adder is having 20.8 % less power than Vedic multiplier with RCA adder at supply vintage 0.9 V.

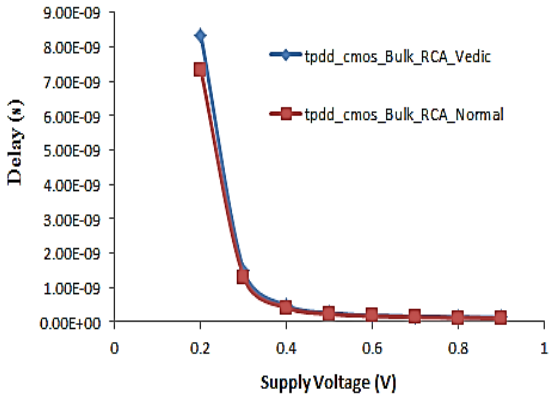

Fig 10: Delay as function of supply voltage

Figure 10 shows the comparison of delay as the function of supply voltage for vedic multiplier and conventional multiplier with RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with RCA adder is faster than the vedic multiplier. Conventional *multiplier with RCA adder is having 13.1 % less delay than vedic multiplier with RCA adder at supply voltage 0.9 V.*

Figure 11 shows the comparison of energy delay product as a function of supply voltage for vedic multiplier and conventional multiplier with RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with RCA adder is having better energy delay product than the vedic multiplier. Conventional multiplier with RCA adder is having 40.2 % energy delay product than vedic multiplier with RCA adder at supply voltage 0.9 V.

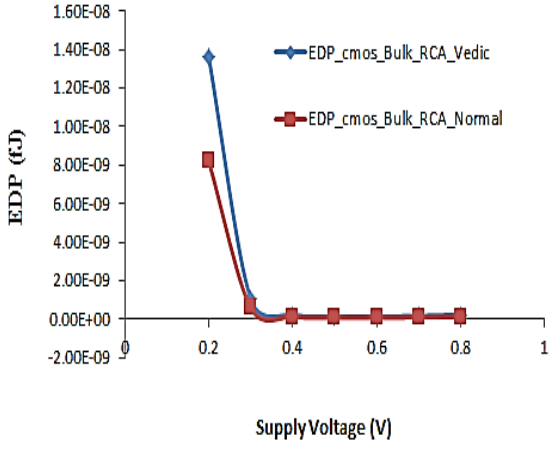

Fig 11: EDP as function of supply voltage

4.1.2 Temp variations

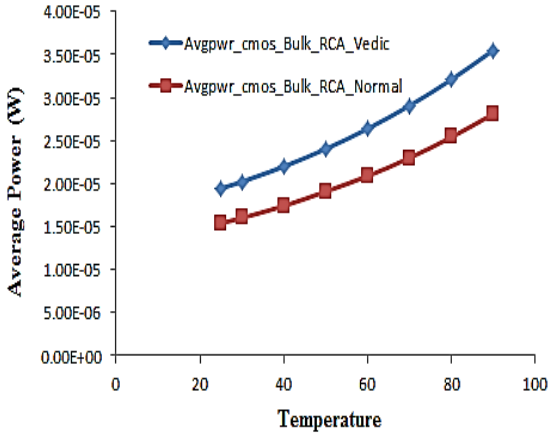

Fig 12: Average power as function of Temperature

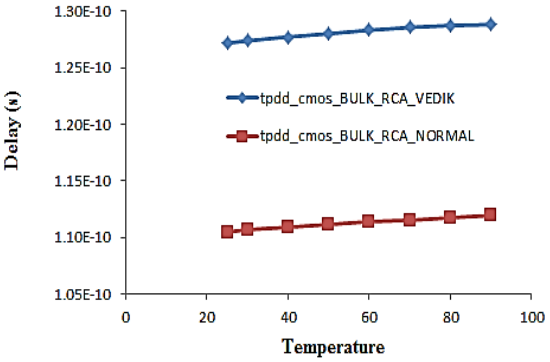

Fig 13: Delay as function of Temperature

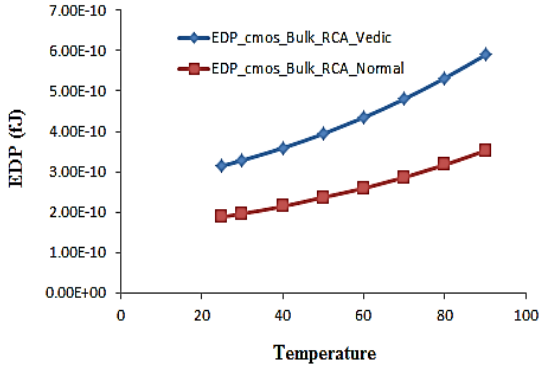

Fig 14: EDP as function of Temperature

Figure 12 shows the comparison of average power as a function of temperature for vedic multiplier and conventional multiplier with RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with RCA adder is more stable over the than the vedic multiplier over the temperature range of 25^0 C to 90^0 C.

Figure 13 shows the comparison of delay as a function of temperature for Vedic multiplier and conventional multiplier with RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with RCA adder is more stable over the than the vedic multiplier over the temperature range of 25^0 C to 90^0 C.

Figure 14 shows the comparison of delay as a function of temperature for vedic multiplier and conventional multiplier with RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with RCA adder is having better EDP than the vedic multiplier over the temperature range of 25^0 C to 90^0 C.

4.2 Conventional and Vedic Multiplier with Carry look ahead adder

4.2.1 V_{DD} variations

Figure 15 shows the comparison of average power as a function of supply voltage for vedic multiplier and conventional multiplier with CLA adder using a bulk device of 32nm. It is observed that the conventional multiplier is having less power than the vedic multiplier. Conventional multiplier with CLA adder is having 23.5 % less power than vedic multiplier with CLA adder at supply voltage 0.9 V.

Figure 16 shows the comparison of delay as a function of supply voltage for vedic multiplier and conventional multiplier with CLA adder using a bulk device of 32nm. It is observed that the conventional multiplier with RCA adder is faster than the vedic multiplier. Conventional multiplier with CLA adder is having 10.3 % less delay than vedic multiplier with CLA adder at supply voltage 0.9 V.

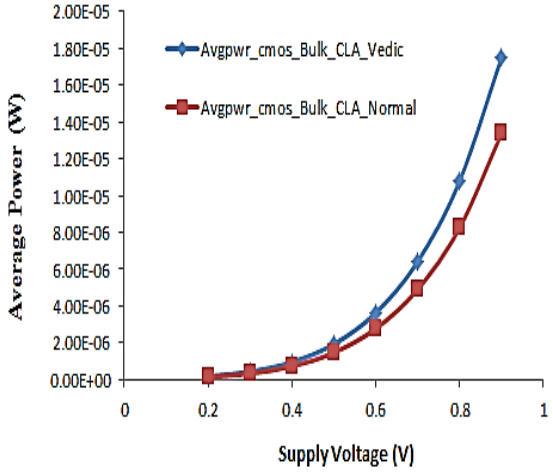

Fig 15: Average power as function of supply Voltage

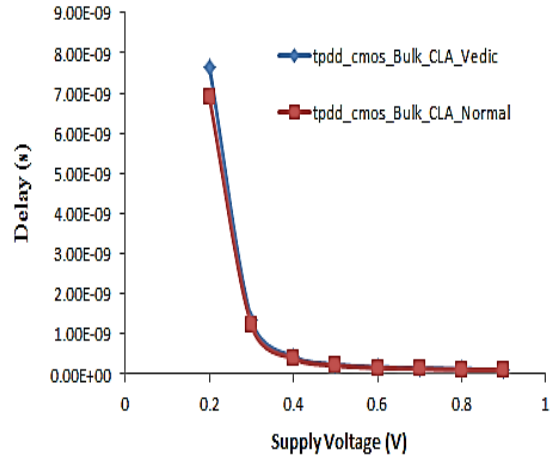

Fig 16: Delay as function of supply Voltage

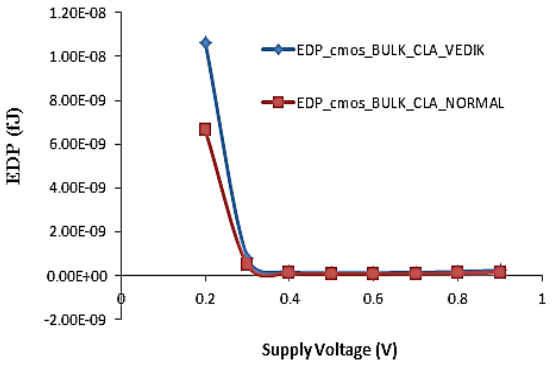

Fig 17: EDP as function of supply Voltage

Figure 17 shows the comparison of energy delay product as a function of supply voltage for vedic multiplier and conventional multiplier with CLA adder using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is having better EDP than the vedic multiplier. Conventional multiplier with CLA adder is having 38.5 % less energy delay product than vedic multiplier with CLA adder at supply voltage 0.9 V.

4.2.2 Temp variations

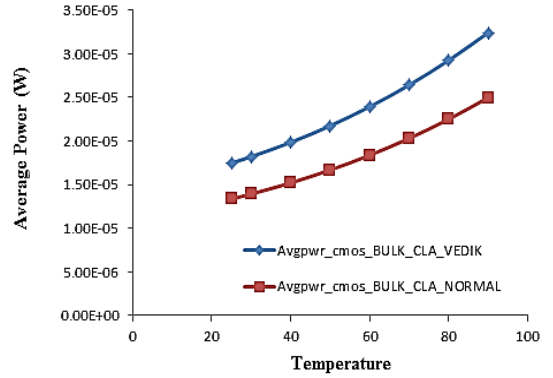

Fig 18: Average Power as function of Temperature

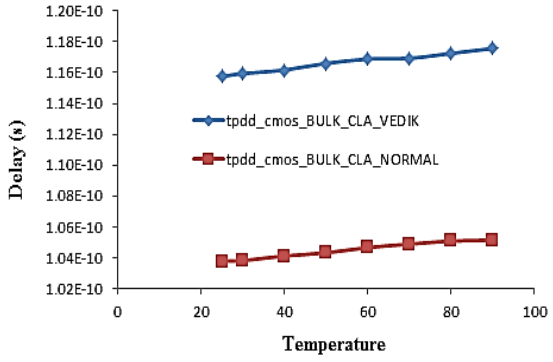

Fig 19: Comparison of delay as function of Temperature

Figure 18 shows the comparison of average power as a function of temperature for vedic multiplier and conventional multiplier with CLA adder using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is more stable over the than the vedic multiplier over the temperature range of 25^0 C to 90^0 C.

Figure 19 shows the comparison of delay as a function of temperature for vedic multiplier and conventional multiplier with CLA adder using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is more stable over the than the vedic multiplier over the temperature range of 25^0 C to 90^0 C. Figure 20 shows mthe comparison of energy delay product as a function of temperature for vedic multiplier and conventional multiplier with CLA adder using the bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is having better EDP than the vedic multiplier over the temperature range of 25^0 C to 90^0 C.m

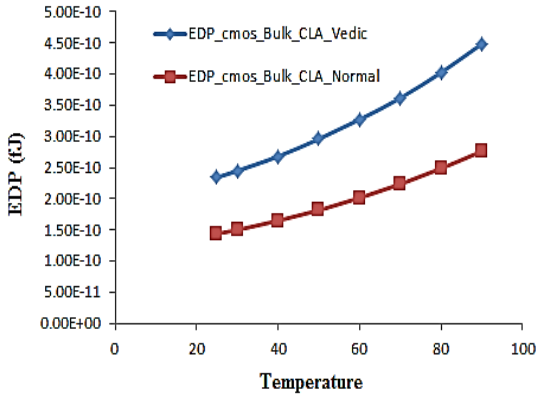

Fig 20: EDP as function of Temperature

4.3 Comparison of Vedic and Conventional Multiplier

4.3.1 V_{DD} variations

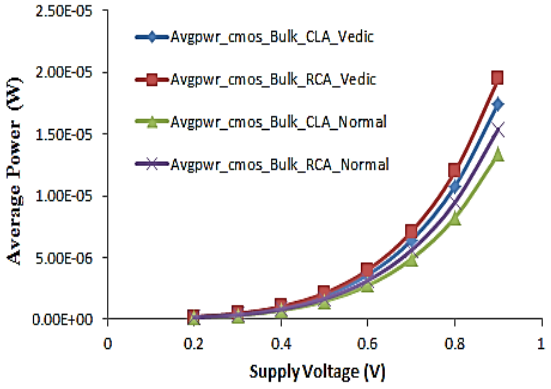

Fig 21: Average power as function of supply Voltage

Figure 21 shows the comparison of average power as a function of supply voltage for vedic multiplier and conventional multiplier with CLA adder and RCA using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is having less power than the rest multiplier. Conventional multiplier with CLA adder is having 45.4% less power than vedic with RCA adder, 30.7 % less than CLA based vedic multiplier and 15.4 % less than conventional multiplier with RCA adder at supply voltage 0.9 V.

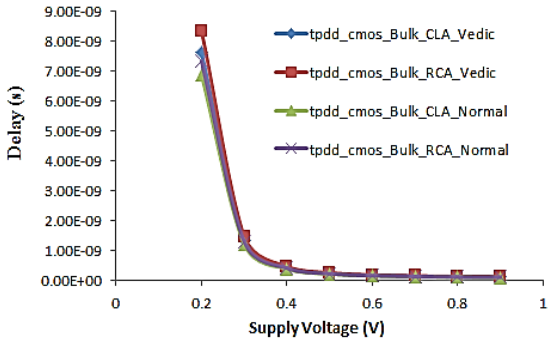

Fig 22: Delay as function of supply Voltage

Figure 22 shows the comparison of delay as a function of supply voltage for vedic multiplier and conventional multiplier with CLA adder RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is faster than the rest multiplier. Conventional multiplier with CLA adder is having 22.5% less delay than vedic with RCA adder, 11.5 % less than CLA based vedic multiplier and 64.7 % less than conventional multiplier with RCA adder at supply voltage 0.9 V.

Figure 23 shows the comparison of energy delay product as a function of supply voltage for vedic multiplier and conventional multiplier with CLA adder and RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is having better EDP than the rest multiplier. Conventional multiplier with CLA adder is having 117 % less energy delay product than vedic with RCA adder, 62.0 % less than CLA based vedic multiplier and 30.7 % less than conventional multiplier with RCA adder at supply voltage 0.9 V.

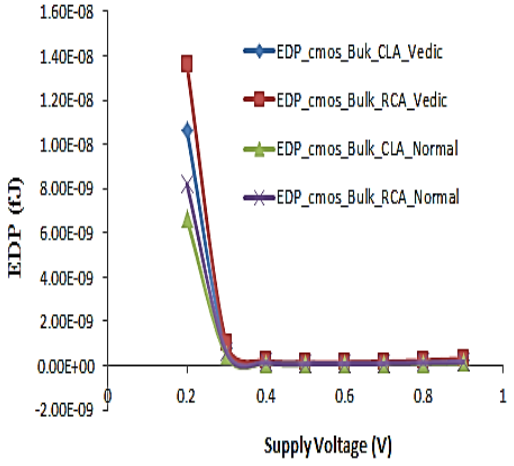

Fig 23: EDP as function of supply Voltage

4.3.2 Temp variations

Figure 24 shows the comparison of average power as a function of temperature for vedic multiplier and conventional multiplier with CLA adder and RCA adder using a bulk device of 32nm.It is observed that the conventional multiplier with CLA adder is more stable over the than the rest multiplier over the temperature range of 25^0 C to 90^0 C. Figure 25 shows comparison of delay as function of temperature for vedic multiplier and conventional

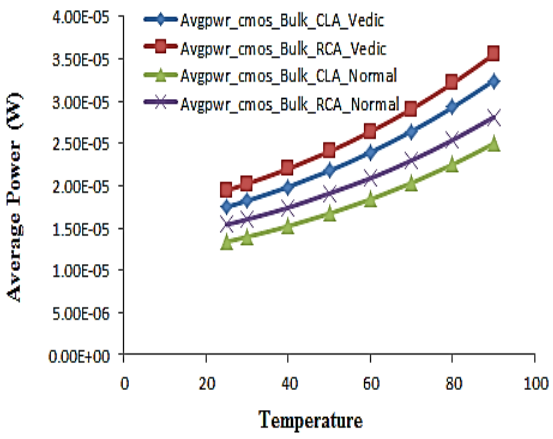

Fig 24: Average power as function of temperature

multiplier with CLA adder is more stable over the than the rest multiplier over the temperature range of 25^0 C to 90^0 C. Figure 26 shows the comparison of Energy delay product as a function of temperature for vedic multiplier and conventional multiplier with CLA adder and RCA adder using a bulk device of 32nm. It is observed that the conventional multiplier with CLA adder is having better EDP than the vedic multiplier over the temperature range of 25^0 C to 90^0 C.

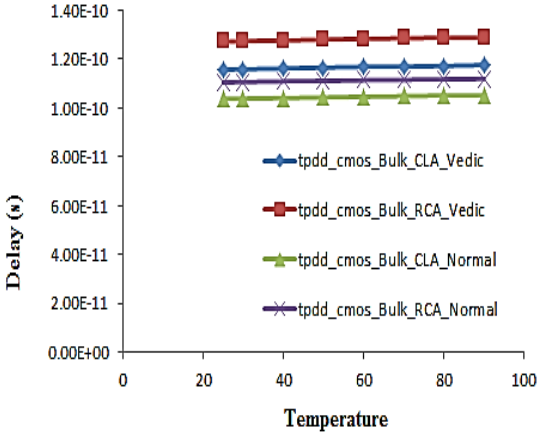

Fig 25: Delay as function of temperature

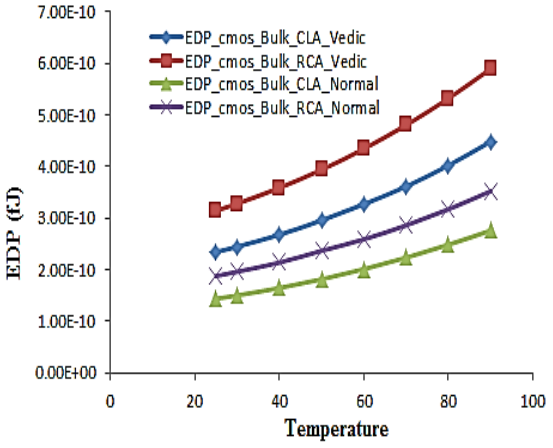

Fig 26: EDP as function of temperature

4.3.3 Process variations

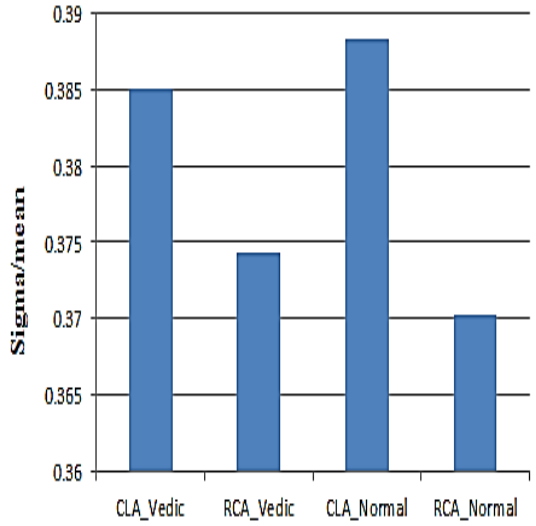

Fig 27: Variation in power with change in process parameter

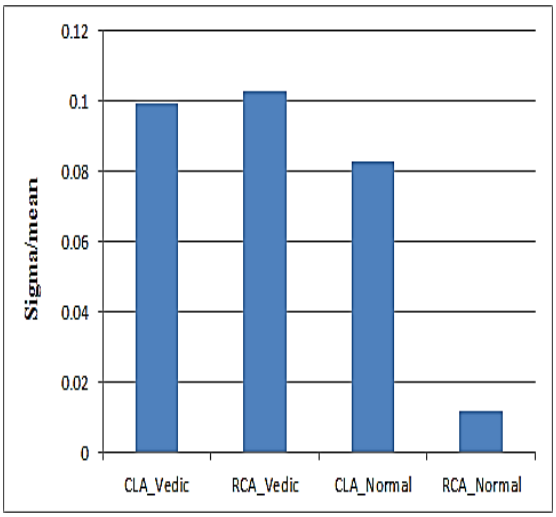

Fig 28: Variation in delay with change in process parameter

Figure 27 and Figure 28 shows Variation in power and delay with a change in process parameter. Monte Carlo analysis has been done on the multiplier. Temperature is varied uniformly with 10 % variation, gate length and threshold voltage changed with 1 sigma rule as Gaussian distribution. The variation shows that RCA normal multiplier is good as per stability is concern.

5. CONCLUSION

Different performance parameters delay, average power, and energy delay product are compared. It is observed that Conventional multiplier with CLA adder is having 45.4% less power than Vedic with RCA adder, 30.7 % less than CLA based Vedic multiplier and 15.4 % less than conventional multiplier with RCA adder at supply voltage 0.9 V. Conventional multiplier with CLA adder is having 22.5% less delay than Vedic with RCA adder, 11.5 % less than CLA based Vedic multiplier and 64.7 % less than conventional multiplier with RCA adder at supply voltage 0.9 V. Conventional multiplier with CLA adder is having 117 % less energy delay product than Vedic with RCA adder, 62.0 % less than CLA based Vedic multiplier and 30.7 % less than conventional multiplier with RCA adder at supply voltage 0.9 V. Conventional multiplier with CLA adder is good over RCA adder based multiplier. These multiplier are useful in the portable devices as a low power and high speed compared to RCA topology.

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