Comparative Analysis of 4x4 Vedic and Conventional Multiplier with different Adders at 32 nm in different Geometrical Devices

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ABSTRACT
Devices optimization for power and speed is a major issue in ultra low power applications. The evolution of the MOSFET has proven to be the best choice for next generation processes. Portable device should have good battery life.Processor speed depends mainly on the multiplier. Paper present the analysis of 4-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) and conventional multiplier with two different adders has been realized using carry look ahead adder and ripple carry adder. Comparative study of multipliers is done for low power requirement and high speed. The main purpose of the paper is to investigate the better adder and multiplication technique. It is observed that the conventional multiplier with Carry look ahead adder is stable and power efficient. Finfet based conventional multiplier with CLA adder is having 10 % less energy delay product than Finfet based VEDIC multiplier with CLA adder and 21.9 % less than FDSOI based conventional multiplier with CLA adder at supply voltage 0.9 V. The variation shows that Finfet based vedic multiplier with CLA adder is having less process variation than fdsoi based conventional multiplier with CLA adder

Keywords
Ripple Carry Adder; vedic multiplier; Energy Delay Product(EDP)

1. INTRODUCTION
One of the major challenges with scaling planar MOSFETs at nanometer region has different issues to design circuits in large SoCs at reduced power consumption levels. The scaling of the devices has been done to accommodate a high number of transistors on the chip. As the devices are scaled down, planar transistors have brought several detrimental effects such as gate oxide tunneling, high leakage currents, and enhancement of Short-Channel-Effects[1]. Several independent studies conducted over the past few decades which has suggested various devices architectures that offer a better solution for short channel effects and allow transistors to shrink below sub100 nm regime. Double-gate MOSFET[2] is becoming an intense subject of VLSI research. It can be scaled to the shortest channel length possible for a given gate oxide thickness. But the difficulty in fabrication of DG MOSFET (Double gate MOSFET) is encountered due to the misalignment of top gate and the back gate[3]. Hence to eliminate the misalignment of gates in DG MOSFET, Finfet[4-5] considered one of the most promising candidates for future generation transistor technologies due to their excellent electrostatic integrity such as Low leakage current, improved short-channel effect and high performance. digital multipliers play significant role in many DSP applications such as fourier transform, filters and in multiplier accumulate unit. Conventional multiplier is array multiplier are in good demand because of their high speed and less power consumption. This multiplier has a regular structure which can be placed one over the another, this reduces layout design and errors.

This work presents a systematic design methodology for 4x4 Vedic multiplier based on Vedic mathematics and conventional multiplier[6]. This implemented using Finfet device and FDSOI device.

This paper is organized in four sections, introduction is given in section I, Section II introduces 4-bit multiplier review, Section III shows simulation results, section IV draws conclusion.

2. 4-BIT MULTIPLIER

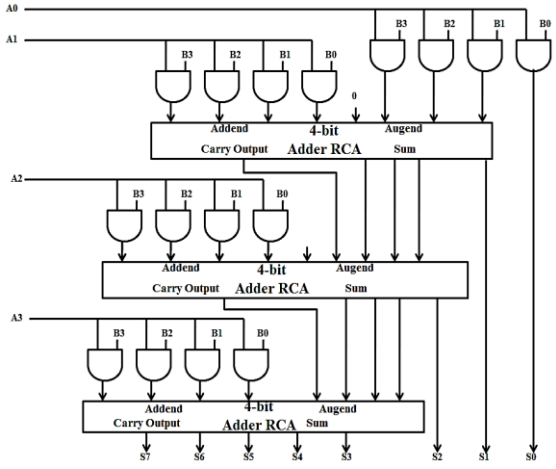

Fig. 1: 4X4 Conventional multiplier

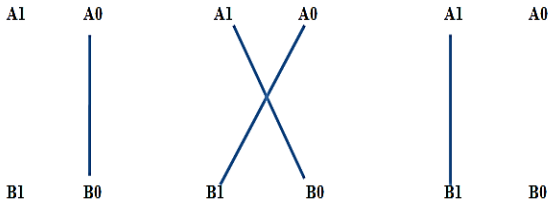

Fig. 2: 2-bit Vedic multiplication

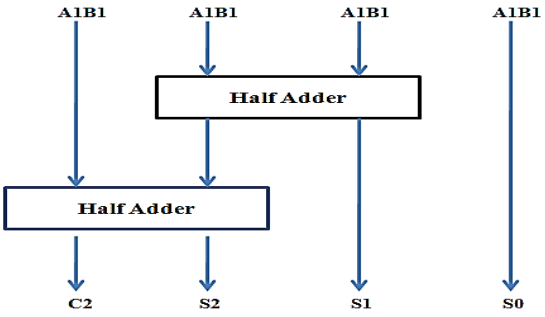

Fig. 3: Block diagram of 2x2 bit Vedic multiplier

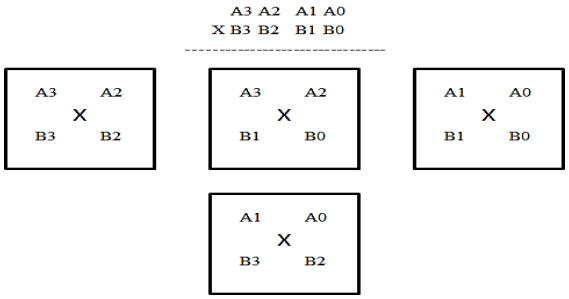

Fig. 4: 4x4 Vedic multiplication

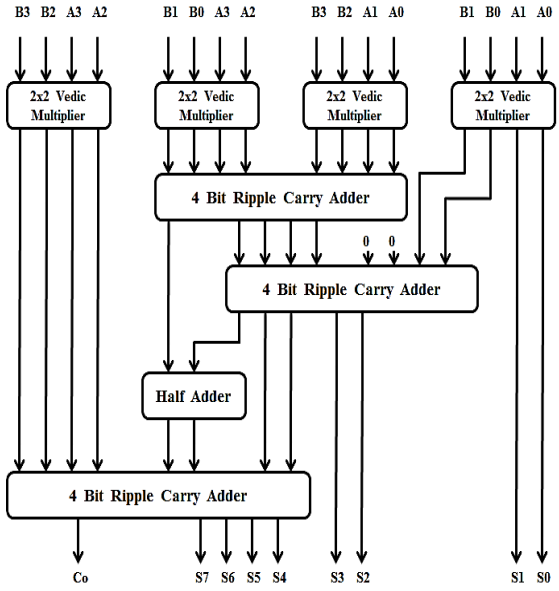

Fig. 5: Block Diagram of 4-bit Urdhva Multiplier with Ripple carry adder

Average power, delay, Energy product delay has been compared for two different adders and multiplier in this paper. Figure 1 shows conventional multiplier with RCA adder same is used replacing CLA adder[7-8]. Figure 2 shows the 2-bit binary number multiplication, figure 3 shows 2x2 multiplier arrangement[9-11]. Figure 4 shows the 4X4 multiplication, same is implemented shown in figure 5 where RCA adder is replaced with CLA adder. All the multiplier has been designed at the transistor level and simulated in H-spice software.

3. SIMULATION RESULTS

3.1. Conventional MULTIPLIER Ripple carry adder and CLA using SOI and FINFET device

3.1.1 VDD variation

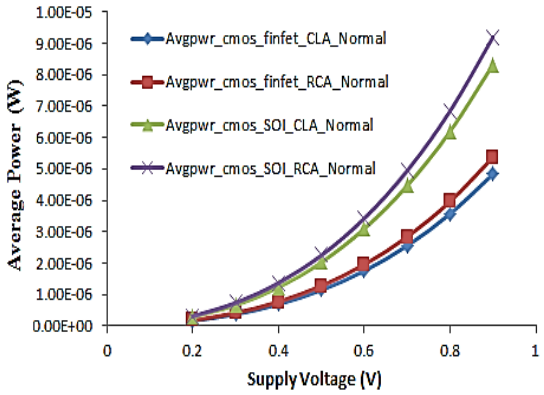

Fig. 6: Comparison of Average Power as function of supply voltage

Figure6 shows comparison of average power as a function of supply voltage. It is observed that the Conventional multiplier with CLA adder in Finfet devices is having less power than another multiplier. Finfet based conventional multiplier with CLA adder is having 9.96 % less power than Finfet based conventional multiplier with RCA adder, 41.9 % less than FDSOI based conventional multiplier with CLAadder and 47.4 % less than FDSOI based conventional multiplier with RCA adder at supply voltage 0.9 V

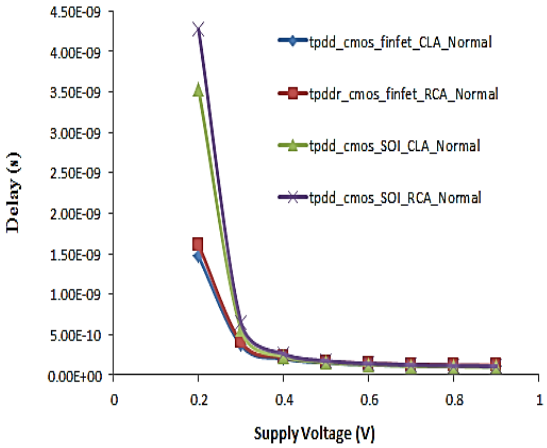

Fig. 7: Comparison of Delay as function of supply voltage

Figure7 shows comparison of delay as function of supply voltage. It is observed that the Conventional multiplier with CLA adder in Finfet devices is faster than another multiplier. FDSOI based conventional multiplier with CLA adder is having 5.86 % less delay than Finfet based conventional multiplier with CLA adder, 13.7 % less than FINFET based conventional multiplier with RCA adder adder and 9.04 % less than FDSOI based conventional multiplier with RCA adder at supply voltage 0.9 V

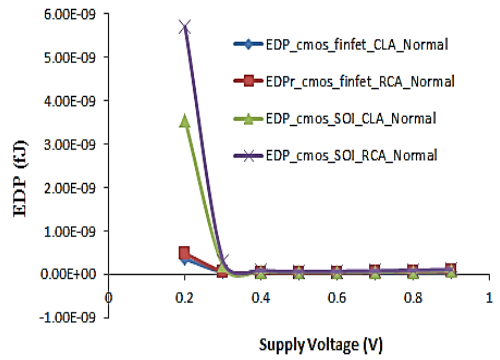

Fig. 8: Comparison of EDP as function of supply voltage

Figure8 shows comparison of energy delay product as function of supply voltage. It is observed that the Conventional multiplier with CLA adder in Finfet devices is having good EDP. Finfet based conventional multiplier with CLA adder is having 24.4 % less energy delay product than Finfet based conventional multiplier with CLA adder, 34.4 % less than FDSOI conventional multiplier with RCA adder and 50.9 % less than FDSOI based conventional multiplier with RCA adder at supply voltage 0.9 V

3.1.2 Temp variations

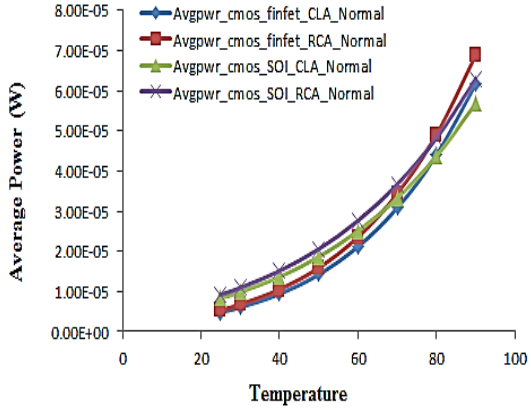

Fig. 9: Comparison of Average power as function of Temperature

Figure9 shows comparison of average power as function of temperature for conventional multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm . It is observed that the conventional multiplier using Finfet device and CLA adder is more stable that the rest over temperature range of 25^0 C to 90^0 C..

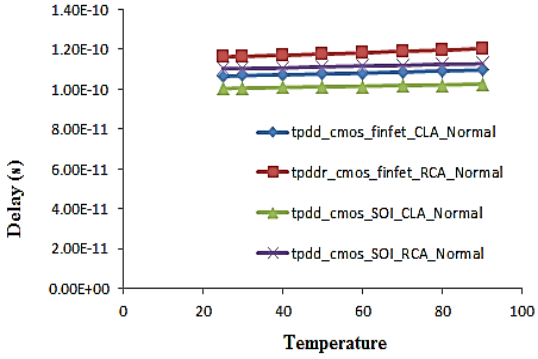

Fig. 10: Comparison of delay as function of Temperature

Figure10 shows comparison of delay as function of temperature for conventional multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm . It is observed that the conventional multiplier using SOI device and CLA adder is faster and more stable.

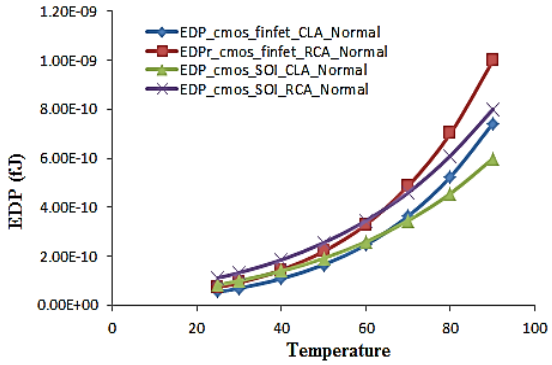

Fig. 11: Comparison of EDP as function of Temperature

Figure 11 shows comparison of EDP as function of temperature for conventional multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm. It is observed that the conventional multiplier using Finfet device and CLA adder is better than the rest multiplier over a temperature range of 25^0 C to 90^0 C.

3.2. Vedic Multiplier RCA and CLA using SOI and FINFET device

Conventional CMOS technique is implemented in all the multiplier with two different technology model file Finfet device and FDSOI device has been used to compare the performance of multiplier. A FDSOI device having gate length 32nm, threshold voltage 0.25V for NMOS and gate length 32nm, threshold voltage -0.29 for PMOS. A Finfet device having same gate length and threshold voltage is used for both NMOS and PMOS. All these parameters have been taken from predictive technology model. Different comparison of delay, power, PDP, EDP has been done in this paper. Figure 4 shows comparison of Delay as function of supply voltage. It is observed that Finfet device is better than the FDSOI device.

3.2.1 VDD variation

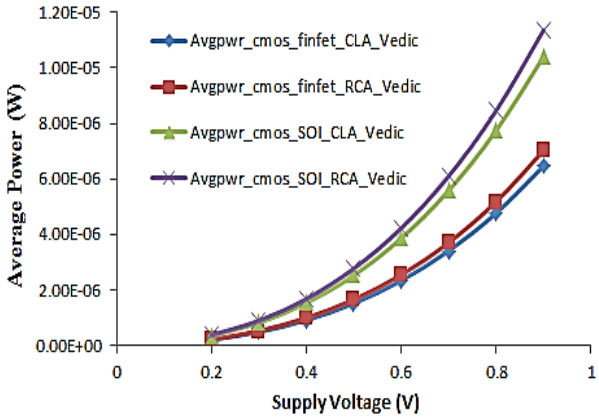

Fig. 12: Comparison of Average power as function of supply Voltage

Figure 12 shows comparison of average power as function of supply voltage for vedic multiplier with RCA and CLA

Adder using Finfet and SOI device of 32nm. is observed that the VEDIC multiplier with CLA adder in Finfet devices is having less power than another multiplier. Finfet based VEDIC multiplier with CLA adder is having 7.9 % less POWER than Finfet based VEDIC multiplier with RCA adder, 37.8 % less than FDSOI based Vedic multiplier with CLA adder and 43 % less than FDSOI based Vedic multiplier with RCA adder at supply voltage 0.9 V

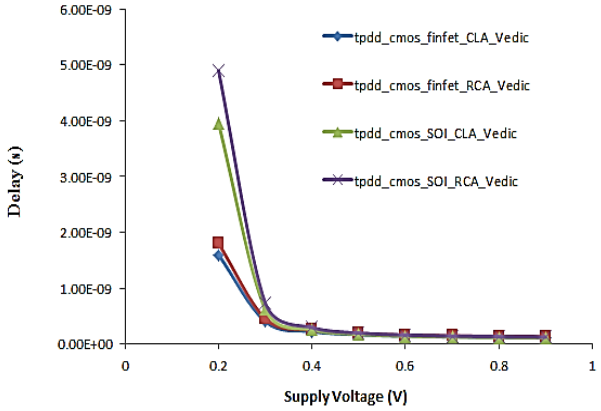

Fig. 13: Comparison of delay as function of supply Voltage

Figure 13 shows a comparison of delay as function of supply voltage for vedic multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm. is observed that the Vedic multiplier with CLA adder in Finfet devices is faster than another multiplier. FDSOI based Vedic multiplier with CLA adder is having 3.69 % less DELAY than Finfet based VEDIC multiplier with CLA adder, 13.7 % less than Finfet based VEDIC multiplier with RCA adder adder and 43 % less than FDSOI based Vedic multiplier with RCA adder at supply voltage 0.9.

Figure 14 shows comparison of EDP as function of supply voltage for vedic multiplier with RCA and CLA Adder

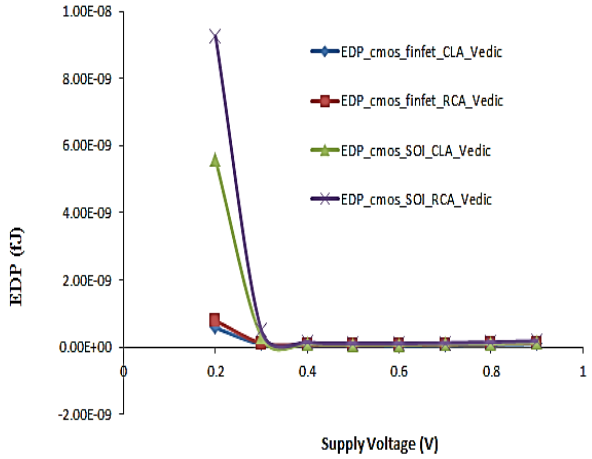

Fig. 14: Comparison of EDP as function of supply Voltage

using Finfet and SOI device of 32nm. is observed that the Vedic multiplier with CLA adder in Finfet devices is much better than another multiplier. Finfet based Vedic multiplier with CLA adder is having 26.10 % less energy delay product than Finfet based VEDIC multiplier with RCA adder, 32.9 % less than FDSOI based VEDIC multiplier with CLAadder and 50.7 % less than FDSOI based Vedic multiplier with RCA adder at supply voltage 0.9 V

3.2.2 Temp variations

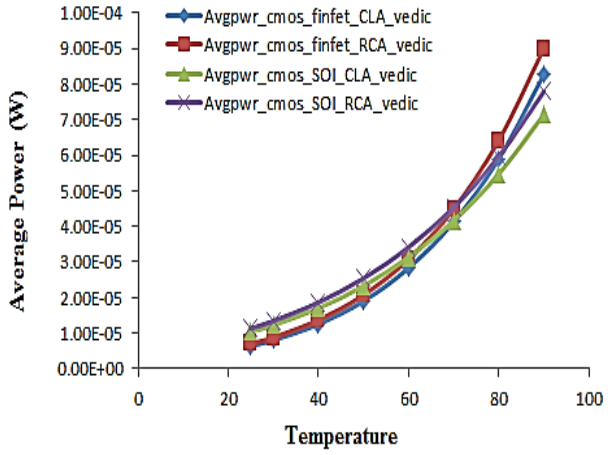

Fig. 15: Comparison of Average Power as function of Temperature

Figure 15 shows comparison of average power as function of temperature for vedic multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm. It is observed that the vedic multiplier using Finfet device and CLA adder is having less power than the rest multiplier over a temperature range of 25^0 C to 90^0 C.

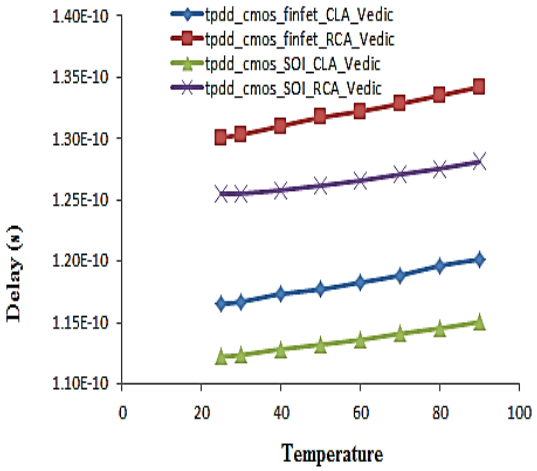

Fig. 16: Comparison of delay as function of Temperature

Figure 16 shows a comparison of delay as function of temperature for vedic multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm. It is observed that the vedic multiplier using SOI device and CLA adder is faster than the rest multiplier over a temperature range of 25^0 C to 90^0 C.

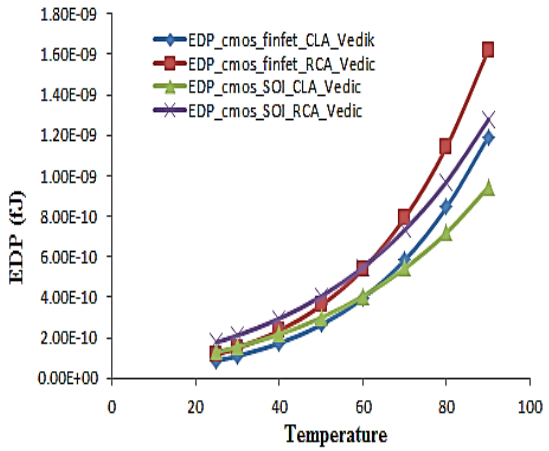

Fig. 17: Comparison of EDP as function of Temperature

Figure 17 shows a comparison of energy delay product as function of temperature for vedic multiplier with RCA and CLA Adder using Finfet and SOI device of 32nm. It is observed that the vedic multiplier using a Finfet device and CLA adder is having better EDP than the rest multiplier over a temperature range of 25^0 C to 90^0 C.

3.3 Comparison of vedic and conventional Multiplier

From the result drawn in section-III, it has been considered to take the best multiplier from above. Finfet based conventional multiplier, Vedic multiplier using CLA adder and FDSOI based conventional multiplier using CLA adder has been considered.

3.3.1 VDD variations

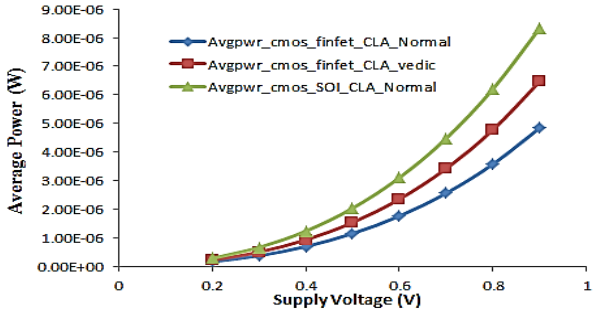

Fig. 18: Comparison of Average power as function of supply Voltage

Figure 18 shows comparison of average power of Finfet based conventional multiplier with CLA adder, Finfet based VEDIC multiplier with CLA adder and FDSOI based conventional multiplier with CLA adder. Finfet based conventional multiplier with CLA adder is having 25.10 % less power than Finfet based VEDIC multiplier with CLA adder and 41.9 % less than FDSOI based conventional multiplier with CLAadder at supply voltage 0.9 V

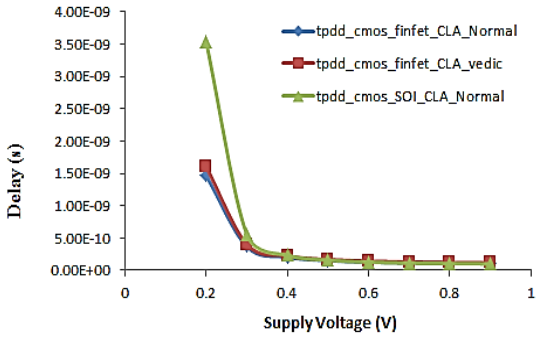

Fig. 19: Comparison of delay as function of supply Voltage

Figure 19 shows comparison of delay of Finfet based conventional multiplier with CLA adder , Finfet based VEDIC multiplier with CLA adder and FDSOI based conventional multiplier with CLA adder. FDSOI based conventional multiplier with CLA adder is having 5.86 % less delay than Finfet based conventional multiplier with CLA adder and 13.9 % less than Finfet based VEDIC multiplier with CLAadder at supply voltage 0.9 V

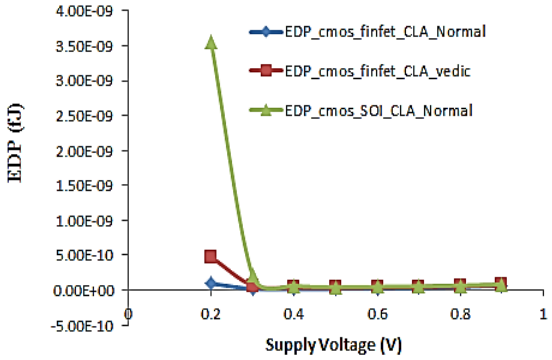

Fig. 20: Comparison of EDP as function of supply Voltage

Figure 20 shows comparison of Energy-delay product of Finfet based conventional multiplier with CLA adder, Finfet based VEDIC multiplier with CLA adder and FDSOI based conventional multiplier with CLA adder. Finfet based conventional multiplier with CLA adder is having 10 % less energy delay product than Finfet based VEDIC multiplier with CLA adder and 21.9 % less than FDSOI based conventional multiplier with CLAadder at supply voltage 0.9 V

3.3.2 Temp variations

From figure 15, figure 16 and figure 17, it is cleared that the Finfet based conventional multiplier using CLA adder, Finfet based Vedic multiplier using CLA adder and FDSOI based conventional multiplier using CLA adder are having comparative same changes in it. But Finfet based conventional multiplier using CLA adder shows less power, delay and energy-delay product.

3.3.3 Process variation

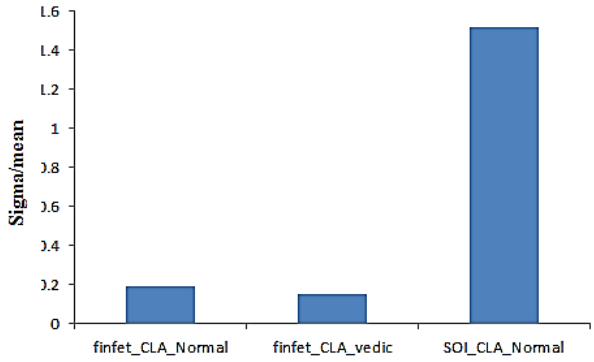

Fig. 21: Variability issues of multiplier

Figure 21 shows variation in power and delay with change in process parameter. Monto Carlo analysis has been done on the multiplier. Temperature is varied uniformly with 10 % variation, gate length and threshold voltage changed with 1 sigma rule with Gaussian distribution. The variation shows that Finfet based Vedic multiplier with CLA adder is having less process variation than FDSOI based conventional multiplier with CLA adder. Finfet based conventional multiplier and Vedic multiplier with CLA adder are have nearly equal variations.

4. CONCLUSION

In this paper Comparison of average power of Finfet based conventional multiplier with CLA adder , Finfet based VEDIC multiplier with CLA adder and FDSOI based conventional multiplier with CLA adder. Finfet based conventional multiplier with CLA adder is having 25.10 % less power than Finfet based VEDIC multiplier with CLA adder and 41.9 % less than FDSOI based conventional multiplier with CLA adder at supply voltage 0.9 V. Comparison of delay of Finfet based conventional multiplier with CLA adder, Finfet based VEDIC multiplier with CLA adder and FDSOI based conventional multiplier with CLA adder. FDSOI based conventional multiplier with CLA adder is having 5.86 % less delay than Finfet based conventional multiplier with CLA adder and 13.9 % less than Finfet based VEDIC multiplier with CLA adder at supply voltage 0.9 V. Comparison of Energy-delay product of Finfet based conventional multiplier with CLA adder , Finfet based VEDIC multiplier with CLA adder and FDSOI based conventional multiplier with CLA adder. Finfet based conventional multiplier with CLA adder is having 10 % less energy delay product than Finfet based VEDIC multiplier with CLA adder and 21.9 % less than FDSOI based conventional multiplier with CLA adder at supply voltage 0.9 V. The variation shows that Finfet based vedic multiplier with CLA adder is having less process variation than fdsoi based conventional multiplier with CLA adder. Finfet based conventional multiplier and vedic multiplier with CLA adder are have nearly equal variations. It is good to use Finfet based conventioanl multiplier with CLA adder for portable applications.

5. REFERENCES

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