Abstract

As the compactness of system-on-chip (SoC) increase, it becomes striking to integrate dedicated test logic on a chip. Starting with a broad idea of test problems, this survey paper focus on “Chip” Built in Self-Test (BIST) study and its promotion for board and system-level applications. This paper gives brief informative review of Built-in Self-test (BIST) and its testing techniques. Recently BIST Research is being highly used in VLSI and SoC testing for the detection fault coverage.

References

concurrent BIST with Low hardware overhead.”


5. B. C. and M. Lubaszewski, “ON-LINE AND OFF-LINE TESTING: FROM DIGITAL TO ANALOG, FROM CIRCUITS TO BOARDS,” IEEE, p. 34.


7. J. Jahangiri and R. Press, “Test patterns for ICs that are both secure and have very high coverage,” AUTOTESTCON (Proceedings), no. September, pp. 92–96, 2008.


**Index Terms**

Computer Science

Software Engineering

**Keywords**

Built-in Self-test, Circuit under test, Device under test, IC, SOC, CTL, PRNG, CRC.