Comparative Analysis of Various Domino Logic Circuits for Improvement of Power and Delay Calculation

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ABSTRACT
The urge of high performance and dynamic functionalities in an integrated circuit has led to aggressive technology scaling over the years. The supply voltage (V_{DD}), device threshold voltage (V_{th}) and the device geometry are expected to be scaled further with this trend. Which results in reducing the short channel effects and increased transistor OFF- state current (I_{OFF}). Additionally leakage currents, higher operating frequency and on die transistor count will lead to increase in total power dissipation. Dynamic logic technique is preferred over static logic technique for the higher performance circuit due to lesser delay which enhances the speed of the circuit and overall capacitance is low compare to CMOS which reduces the power consumption. In this paper we have calculate the Average power consumption and delay of various domino circuits provided with 8 input OR gate, comparison of power, delay, and Unit Noise Gain (UNG) of different topologies. The simulation is performed in HSPICE at 65nm and 45nm process technology with supply voltage 1V and 0.9V and operating temperature of 27^0 C at 100 MHz for fair comparison of results. We have also calculated the power consumption and delay with the variation of keeper ratio in all the existing technique at 65nm and 45nm process technology.

Keywords
Domino Logic, High speed, Low power, UNG

1. INTRODUCTION
Conventional VLSI Designers have different options to reduce the power of the circuit for their designs. But the current semiconductor industry using a millions of transistor on small area which is invoking the new sources of power consumption such as leakage current in standby mode of transistor. There are many approaches to reduce the power dissipation of the circuit at various design stages and different design techniques have been proposed. However, scaling of technology leads to achieve higher density and performances in digital circuits. As a concerns, the leakage current which is flow in nanometer regime (e.g. Short Channel Devices (SCD)) becoming a dominating part of total power dissipation in CMOS circuit. To reduce dynamic power dissipation it is necessary to reduce the supply voltage of the circuit, reduction of supply voltage after a certain limit affects the performance of the circuit [1-2], to maintain circuit performance of the circuit it is necessary to decrease the threshold voltage as well, but it leads to leakage power dissipation. Leakage power can be reduced by increasing the threshold voltage [3]. In this paper the leakage current is reducing in pull down network on the Circuit. For the suggested technique uses Two PMOS in Pull Down network [4].

The CMOS technology has become very important in VLSI circuit designs. Since now a day's nearly all the electronics devices and integrated circuits are fabricated using this technology. In a CMOS circuit design we use a complimentary pair of NMOS and PMOS transistors with the metal oxide layer on the top of the semiconductor bar. Thus CMOS abbreviated as Complementary Metal Oxide Semiconductor. The NMOS and PMOS are in compliment form in the CMOS technology. Whenever one of the transistors is ON, the other transistor will be automatically OFF. Consequently the current cannot pass directly from supply to the ground. Hence the power dissipation in CMOS is minimum compared to all logic families [5-7].

Properties

- A transistor operates as a 'switch' controlled by its gate.
- PMOS transistors are used to construct the PUN; while the NMOS devices construct the PDN.
- Parallel connected NMOS transistors represent an OR function; series connected NMOS transistors represent an AND function.
- 2N numbers of transistors are required to implement an N-input logic.
- Only non-inverting structures are possible because of the presence of inverting buffer.
- Charge distribution may be a problem.

The rest of the paper is arranged as follows. Section II, studies seven types of circuits that have been proposed in related literatures, standard footless domino logic, standard footed domino logic, Conditional keeper, high speed, Diode footed, Leakage current Replica, Current comparison Domino Logic circuit. Simulation results of different methods explained in section II is compare. In section III comparison includes delay, power, Unit Noise Gain (UNG) of all the existing technique is done for calculation of overall performance and conclusion is offered in section IV.

2. LITERATURE REVIEW
In the literature survey, the various types of domino logic configurations are shown:

[1] Kaushik Roy et. al., 2003 [3], "Reviewed all causes of leakage current in transistor that includes gate Subthreshold current which is the main source of power consumption which depend upon DIBL, width of the transistor, temperature, etc. gate-oxide tunneling which increases the leakage current when geometry of the device is reduces.

[2] Ali Peiravi and M. Asyaei, 2012 [10], "Robust low leakage controlled keeper by current comparison Domino (CCD) which is used in wide fan-in gates for calculation of UNG" presents various domino logic circuits. The main focus behind this approach is to reduce the contention current

between the keeper transistor and evaluation network for increasing the performance of the circuit performance using current comparison between the leakage current due to the low level inputs and the current due to at least one input at high level.

[3] Farshad Moradi, TuanVu Cao, ElenaI.Vatajelu, Ali Peiravi, Hamid Mahmoodi, Dag T. Wisland, 2012 [2], "The proposed technique uses the difference and the comparison between the leakage current of the OFF Transistors. The Pseudo NMOS logic is used to generate carry and pass transistor is used to generate sum. To reduce static and total power dissipation, additional ALD (Active Level Driving) circuit is used to activate pull-up PMOS transistor.

[4] Ali Peiravi and Mohammad Asyaei 2013[14], In this paper, a new domino circuit is proposed which has a lower leakage and higher noise immunity without dramatic speed degradation for wide fan-in gates. The technique which is utilized in this paper is based on comparison of mirrored current of the pull-up network with its worst case leakage current. The proposed circuit technique decreases the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement fast and robust circuits. Thus, the contention current and consequently power consumption and delay are reduced.

(a) Footless Standard Domino Logic & Footed Standard Domino Logic

In basic domino circuit standard footless domino logic and footed domino logic come into the existence which is shown in Figure 1 & 2. In standard domino logic circuit design, for reduction of contention current problem a keeper transistor is used which is drive by output of the inverter circuit to maintain the proper charge over the dynamic node. But the resulting contention between the keeper transistor and pull down networks reduces the power and speed characteristics of the circuit [7]. In standard footerless domino logic, the feedback keeper transistor is parallel with the pre-charge transistor, the keeper transistor is a week transistor to reduce the charge sharing problem and contention current problem when circuit enter into the evaluation phase.[8-9]. Keeper transistor causes lots of contention problem, when the PDN gets ON through evaluation phase, which results in slower gate performance. When we design a high fan-in gate with deep submicron technology; we need a very strong keeper transistor to compensate the large amount of leakage current flowing through the PDN of the logic gate. Static CMOS performs very well in terms of robustness and energy, but is not good in terms of delay. Domino CMOS logic performs very well in terms of delay, but is not good in terms of robustness and energy. A slight noise present in the input of the domino logic modifies the output logic level. In domino logic style present a static CMOS inverter at the output of the dynamic node. Due to this, noise immunity of the circuit increases and capacitance at the output node reduces. In this thesis, as we proceed further, we have proposed a novel circuit technique for domino logic.

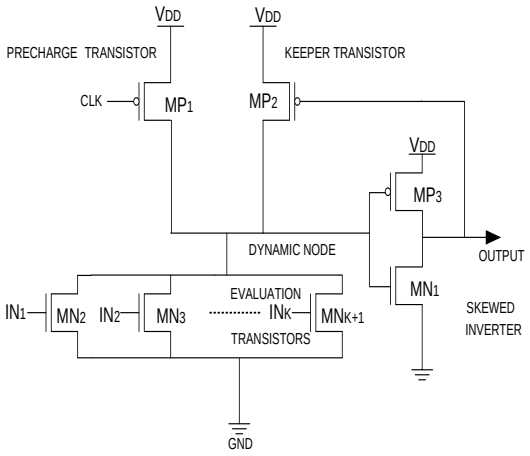

Figure 1: Standard Footerless Domino Logic Circuit

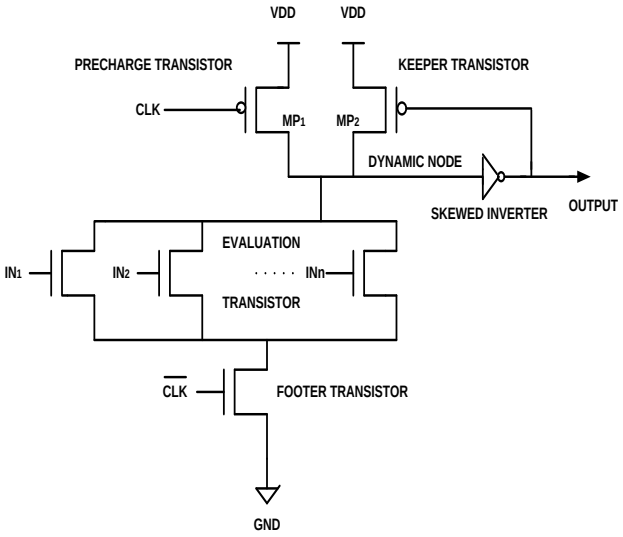

Figure 2: Standard Footed Domino logic circuit

(b) Conditional Keeper Domino Logic

In this technique the two keeper transistor are introduce K1 and K2 week and strong keeper to reduce the contention current problem the keeper K1 is strong keeper which is activate when circuit enter into the evaluation phase the delay is provided to the keeper with NAND gate circuit for reduction of power consumption and enhance the noise immunity of the circuit. The work in two phase pre-charge and evaluation phase, during pre-charge phase K2 keeper play a major role in reduction of power consumption and during evaluation phase K2 keeper come into the existence as shown in Figure 3. The only drawback of this circuit is that large number of transistor is used so areas overhead take place [7].

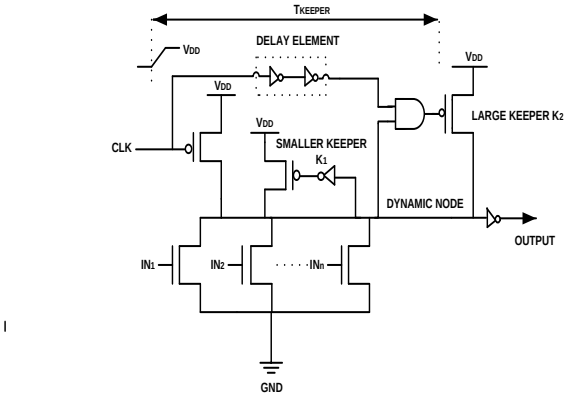

Figure 3: Conditional Keeper Domino Logic

(c) High Speed Domino Logic

Another type of domino circuit is known as High speed domino in this configuration a reduction of delay take place shown in Figure 4. High speed domino circuit also work in two phase pre-charge and evaluation phase during pre-charge phase MP1 transistor turns ON and MP3 also turns ON initially keeper transistor turns OFF for reduction of the delay of the circuit. When circuit enter into evaluation phase keeper transistor turns ON with the help of MN1 transistor, MN1 transistor is a pass transistor which reduces the overall area of the circuit and reduces the delay of the circuit for faster operation of the circuit in DSM technology[10].

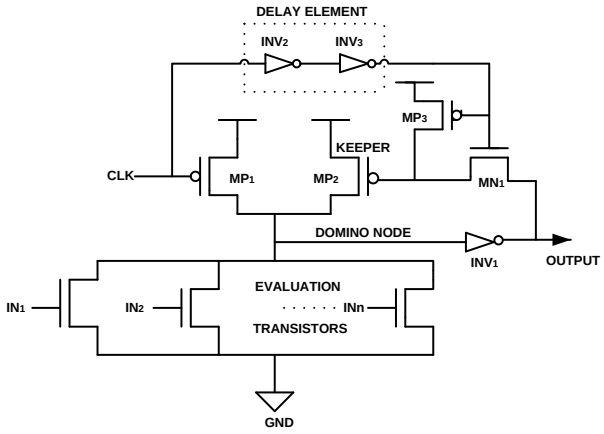

Figure 4: High-Speed Domino Logic

(d) Diode Footed Domino Logic

Another type of domino circuit design is Diode footed which is the most prominence technique for mitigation of power consumption and enhances the UNG of the circuit [11-13]. Here the change is done in the evaluation network a mirror transistor is inserted below evaluation network as shown in Figure 5. While we can't stop the pre-charge phase of the domino logic, we can certainly minimize pulses at the output, thus we can improve the domino circuit in order to reduce noise and power consumption. In this thesis, we have made adopted a novel approach to mitigate this problem. Circuit proper logic as shown in Figure 6.

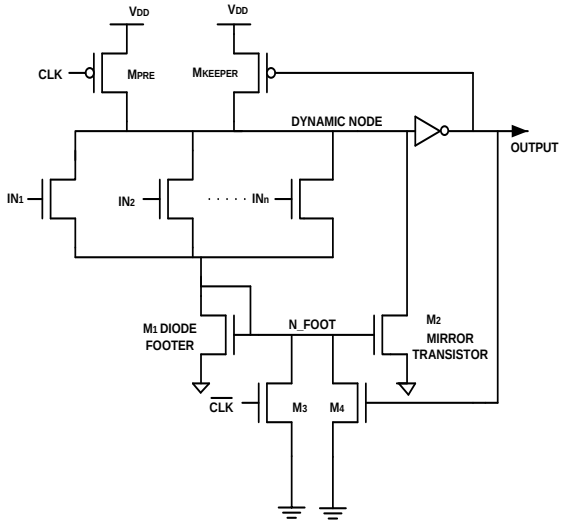

Figure 5: Diode Footed Domino Logic Mirror ratio is formulated by:

$$M=\frac{(W/L)\ \text{mirror transistor}}{(W/L)\ \text{footer transistor}} \qquad (1)$$

As we increase the mirror ratio performance will increase but at the cost of decreased robustness.

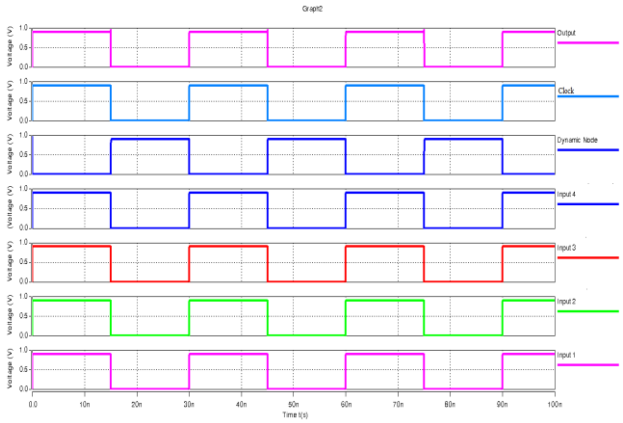

Figure 6: Transient characteristics of 4-input proposed domino OR gate using HSPICE

3. PERFORMANCE COMPARISON OF PRESENTED METHODES

All the simulations are performed in 65 nm and 45nm technologies with operating frequency at 100MHz and V_{DD} of 1V and 0.9V by using HSPICE simulator. For calculation of delay of the circuit fall/rise times of the waveforms were set to 1pS. Considering the application of wide OR gates delay, power dissipation and UNG (Unit Noise Gain) is calculate for wide Fan-in 8 input OR gate for all the existing techniques for reduction of power consumption. Table I. indicates the power and delay calculation at 65nm and 45nm technology. Figure 7 to 11 shows the all the parameters like power, delay, PDP, UNG is calculated for all existing technique at 65nm and 45nm technology, area of the circuit is calculated with number of transistor. Table II and III shows the variation of keeper ratio in power consumption and delay calculation.

For calculation of UNG [11], a pulse noise is applied to all inputs with amplitude which is a fraction of supply voltage and a pulse width equal to 50% of duty cycle. Then, the

amplitude of the input noise pulse is increased and measure the amplitude of output if input and output amplitude is equal voltage is equal this is called the UNG of the circuit. This noise amplitude of the circuit is defined as

UNG= [V_{in},V_{noise} = V_{output}]

Table 1. Power and delay performance of 2-input OR gate using 65nm and 45nm technologies

Tech	Power	Delay	PDP
65nm	5.10 E-6	25.89 E-12	132.09E-18
45nm	3.20 E-6	23.90 E-12	76.48E-18

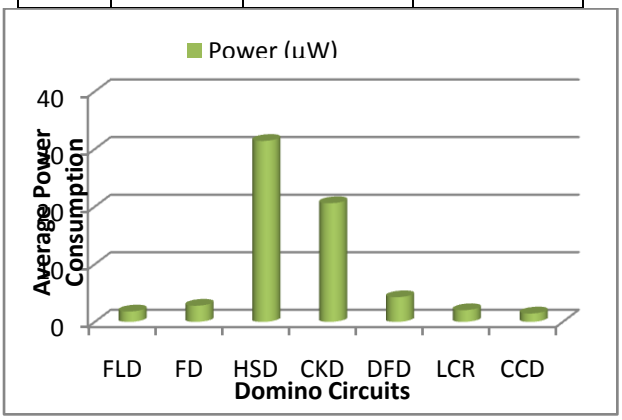

Figure.7: Average Power Consumption for 8 Inputs OR Gate at 65nm

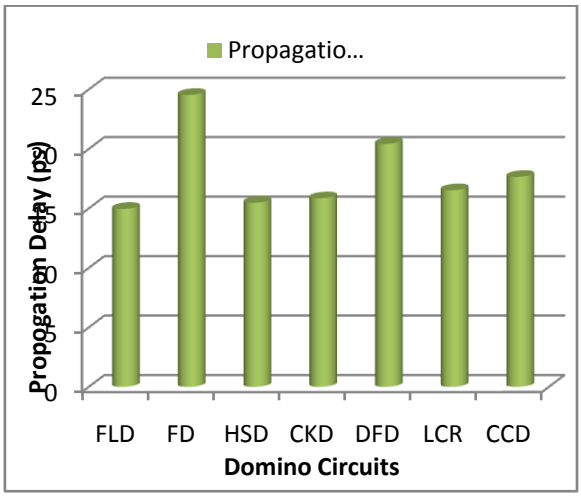

Figure.8: Propagation Delay for 8 Inputs OR Gate at 65nm

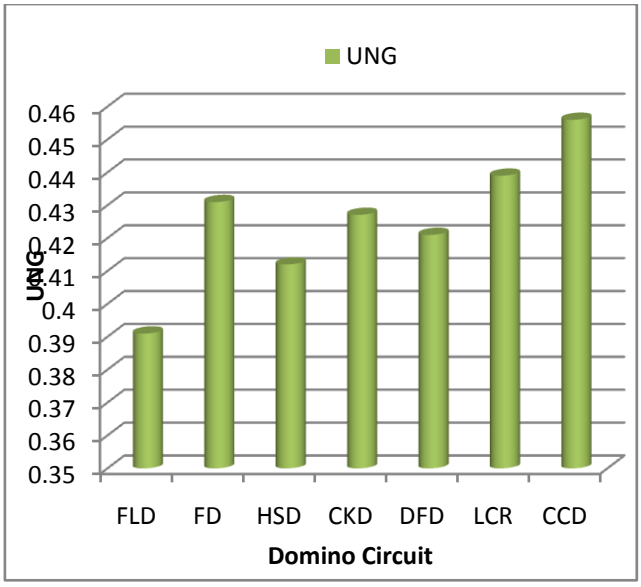

Figure.9: UNG for 8 Inputs OR Gate at 65nm

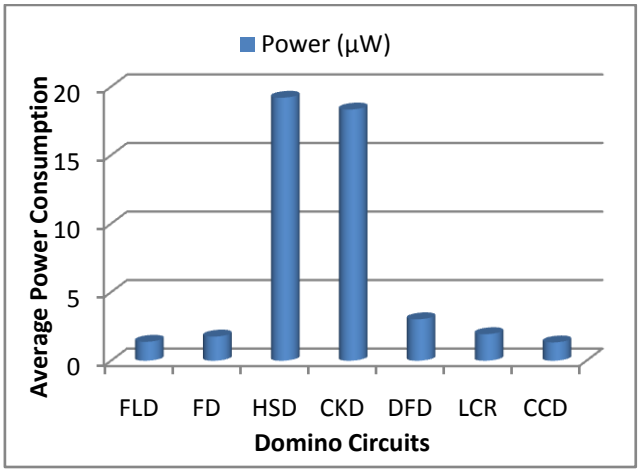

Figure.10: Average Power Consumption for 8 Inputs OR Gate at 45nm

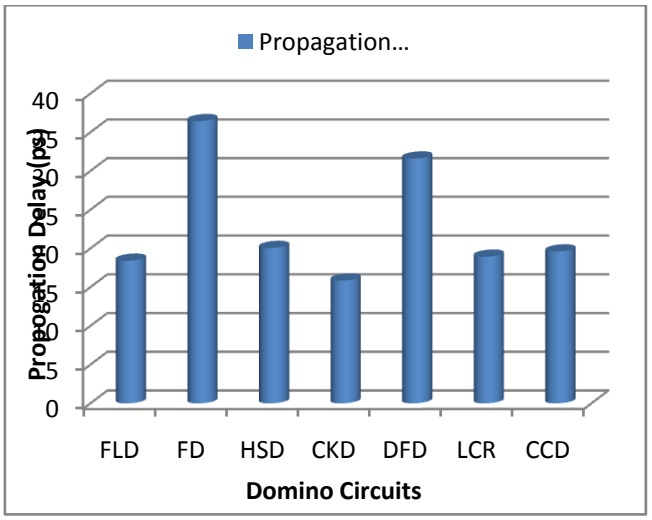

Figure.11: Propagation Delay for 8 Inputs OR Gate at 45nm

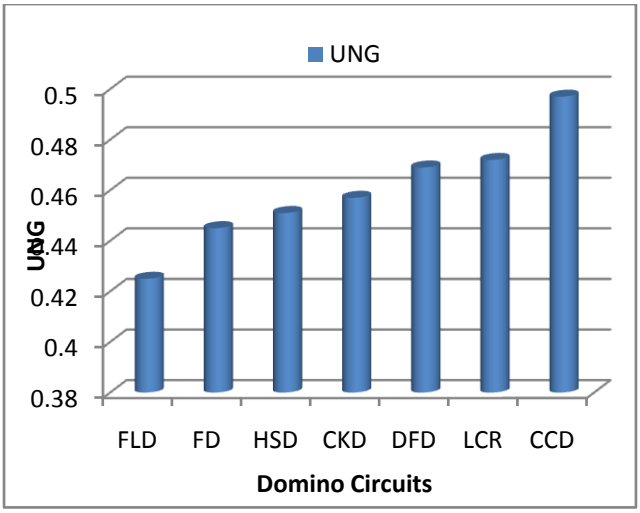

Figure.12: UNG for 8 Inputs OR Gate at 65nm

4. CONCLUSION

In the nanoscale CMOS technology, leakage loss is major concern. The focus of this dissertation is the problem of increasing leakage in modern VLSI designs. In this dissertation we have studied various domino techniques for low power VLSI design. On the other hand this increased threshold voltage improves the noise immunity. At 25^0C the active power consumption decreases by 44.45% in AND2, 13.66% in OR2, 16.02% in OR4, and 18.33% in OR8; at 110^0C it decreases by 33% in AND2, 12.06% in OR2, 12.78% in OR4, and 14.3% in OR8 when compared with standard footerless domino circuits. The whole simulation and comparison is based upon 65nm CMOS technology using HSPICE. It is expected that it can be an extremely fruitful line of future research. Moreover, proposed techniques for domino circuits can be used in carbon nano-tubes technology for better performance in real world systems.

5. REFERENCES

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