A Multilevel Inverter System for an Induction Motor with Open-Ended Windings

V. Srinath
Research Scholar
Dayalbagh educational Institute, Agra

Man Mohan
Professor
Dayalbagh educational Institute, Agra

D. K. Chaturvedi
Professor
Dayalbagh educational Institute, Agra

ABSTRACT
The objective of this paper is to present a multilevel inverter topology for induction motor with open-end winding. Multi level inversion is achieved by feeding an open-end winding induction motor with a two-level inverter in cascade with three auxiliary circuits from one end and a single two-level inverter from the other end of the motor. The combined inverter and auxiliary system with open-end winding induction motor produces voltage space-vector location identical to five-level inverter. The proposed inverter drive scheme was simulated for different type of loads and also with sudden changes in the load. It is also capable of producing a multilevel pulse width modulation (PWM) waveform to a five level depending on the modulation range. The proposed topology has been simulated using MATLAB/SIMULINK with satisfactory results.

General Terms
Multilevel Inverter, Open ended winding Induction motor

Keywords
Auxiliary circuit, Induction motor, multilevel inverters, open-end winding, pulse width-modulation strategy.

1. INTRODUCTION
Multilevel inverters have been used widely because of their high power capability, lower output harmonics and lower commutation losses etc.. Multilevel inverters have the main advantages that the harmonic components of line-to-line voltage fed to load, switching frequency of the devices and electromagnetic interface (EMI) problem could be decreased. They can also reduce the stress on the switching devices as higher levels are synthesized from voltage sources with lower levels. These features have made them suitable for application in large and medium induction motor drives. There are four main topologies of multilevel inverters relevant for large induction motor drive applications: the neutral point clamped inverters, cascaded H-bridge inverters, flying capacitor multilevel inverters and open-end winding induction motor fed by dual inverters [1]-[9]. In recent years, many multilevel inverters synthesizing a large number of levels and their applications have been reported [7]–[27].

In series-connected H-bridge topology of multilevel inverter fed induction motor drives, it requires separate DC supply for all the three phases, which increases the power circuit complexity. A five-level inverter structure using the H-bridge topology will require total six power supplies [15,16]. The extended neutral-point clamped inverters experience neutral-point fluctuations as the DC-link capacitors have to carry the load current [16].

Feeding the open-end winding induction motor from both ends also results in a multilevel structure [17]-[22]. The open-end winding structure is realized by opening the neutral-point of the conventional squirrel cage induction motor. The open-end winding induction motor is then fed by two inverters from the two ends of the winding. In [17], a phase-shifted sine–triangle PWM is used for the multilevel voltage generation for the open-end winding induction motor drive and in [18, 20]a space-vector-based PWM approach is explained for three-level voltage-space phasor generation for an open-end winding induction motor drive. In [19] an open-end winding induction motor drive using two 3-level inverters generates a multilevel voltage-space phasor generation, equivalent to a conventional five-level inverter, and the three-level topology used is realized by cascading two 2-level inverters with four DC sources of $V_{dc}/4$, where, V_{dc} is the DC-link voltage of the conventional 2-level inverter fed induction motor drive.

In the present work, a five level inverter system for an open ended induction motor is fed with conventional two-level inverter on both the ends with an auxiliary circuit and two DC sources. Hence, the proposed system does not experience neutral point fluctuations and also uses lesser number of DC sources and switching devices compared to the series-connected H-bridge topology and the existing open end winding induction motor drive using two 3- level inverters [12,16]. In addition to two 2-level inverters feeding the coils of induction motor from both ends, H-bridge cells fed by capacitor are connected in series with the motor winding in each phase to maintain the required level of output voltage [21.22]. Cascade multilevel converter topologies with reduced number of switches for a five and seven level inverter are proposed in [21]-[27]

This paper is organized as follows: Section-II explains the working principle of the proposed five level inverter structure. Multilevel - carrier based PWM scheme is explained in Section-III. The simulation results of the proposed system are discussed in Section-IV. Finally, conclusion is given in Section- V.

2. PROPOSED INVERTER STRUCTURE
The proposed inverter configuration with open-endedwinding induction motor is shown in Fig. 1.

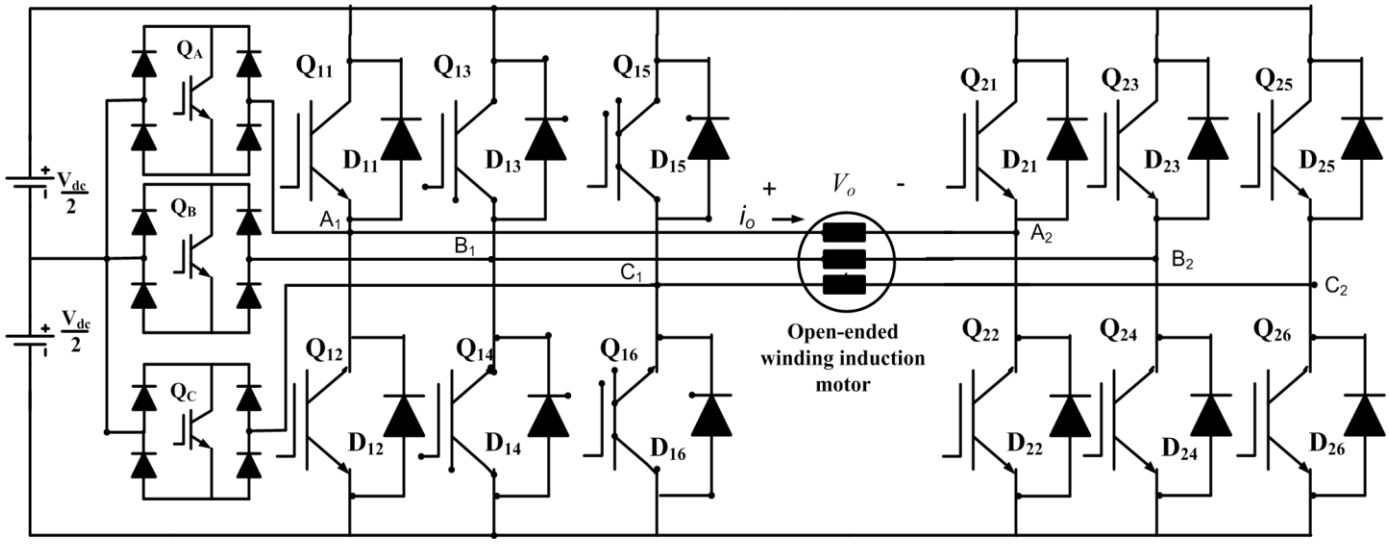

Fig. 1: Proposed power circuit configuration

The induction motor is fed with two 2-level conventional inverters, three auxiliary circuit and two equal DC sources. The auxiliary switch consists of one switching element and four diodes which are connected to the center-tap of the dc power supply. Proper switching control of the auxiliary switch can generate half level of dc supply voltage $+V_{dc}/2$ and $-V_{dc}/2$.

The operation of the proposed structure for phase-A is divided into ten switching states as shown in Fig. 2(a) to Fig. 2(j). The additional switch Q_A, Q_B and Q_C should be properly switched considering the direction of load current. The switching modes and gate signal patterns adopted for the proposed inverter are illustrated in Fig. 3 and Fig. 4 respectively. The output voltage levels according to the switch on-off conditions are shown in Table I.

The switches Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_{15} and Q_{16} belongs to conventional three phase two level inverter-1 and the switches Q_{21}, Q_{22}, Q_{23}, Q_{24}, Q_{25} and Q_{26} belongs to inverter-2. A five level three phase inverter output with open ended winding induction motor is achieved as follows:

From Fig. 2(a) it is observed that when switch Q_{11} and Q_{22} are turned–on, the output voltage V_o will be V_{dc}. The anti parallel diodes across, the switches allow continuous current flowand thus help to maintain asinusoidal output current. When Q_{22} and auxiliary switch Q_A are switched the output voltage will be $V_{dc}/2$ as illustrated in Fig. 2 (c) and (d) respectively.

Further, when the switches Q_A is turned-off and Q_{22} is on the current will flow through the antiparallel diode connected to Q_{12} In this stage the output voltage V_o is zero. For commutation purposes if the switch Q_{12} is turned on and Q_{22} is turned- off then the output voltage will be zero as illustrated in Fig. 2(d) and Fig. 2(f) respectively. Similarly, for achieving $-V_{dc}/2$ and $-V_{dc}$ the switches and the auxiliary circuit is turned-on as per Fig. 2(g), 2(h), 2(i) and 2(j) respectively.

Table I
Operation Stages And Switching Strategy To Realize Five Levels For Phase -A

Switching stages	Fig No	Output voltage V_o	Switches turned-ON	Direction of load current *io*
Stage- 1	2(a)	$+V_{dc}$	Q_{11} and Q_{22}	+
Stage- 2	2(b)	$+V_{dc}$	D_{22} and D_{11}	-
Stage- 3	2(c)	$+V_{dc}/2$	Q_{22} and Q_A	+
Stage- 4	2(d)	$+V_{dc}/2$	D_{22} and Q_A	-
Stage- 5	2(e)	0	Q_{22} and D_{12}	+
Stage- 6	2(f)	0	Q_{12} and D_{22}	-
Stage- 7	2(g)	$-V_{dc}/2$	Q_{21} and Q_A	+
Stage- 8	2(h)	$-V_{dc}/2$	Q_A and D_{21}	-
Stage- 9	2(i)	$-V_{dc}$	Q_{21} and Q_{12}	+
Stage- 10	2(j)	$-V_{dc}$	D_{12} and D_{21}	-

Table I summarizes the various switching stages; output voltage V_o and the direction of load current i_o. The five output voltage levels are obtained by the switch combinations and corresponding stages given in Table II.

Table Ii
Mode Of Operation And Voltage Levels For A-Phase

Mode	I	II	III	IV
High level	V_{dc}	$V_{dc}/2$	0	$-V_{dc}/2$
Low level	$V_{dc}/2$	0	$-V_{dc}/2$	$-V_{dc}$

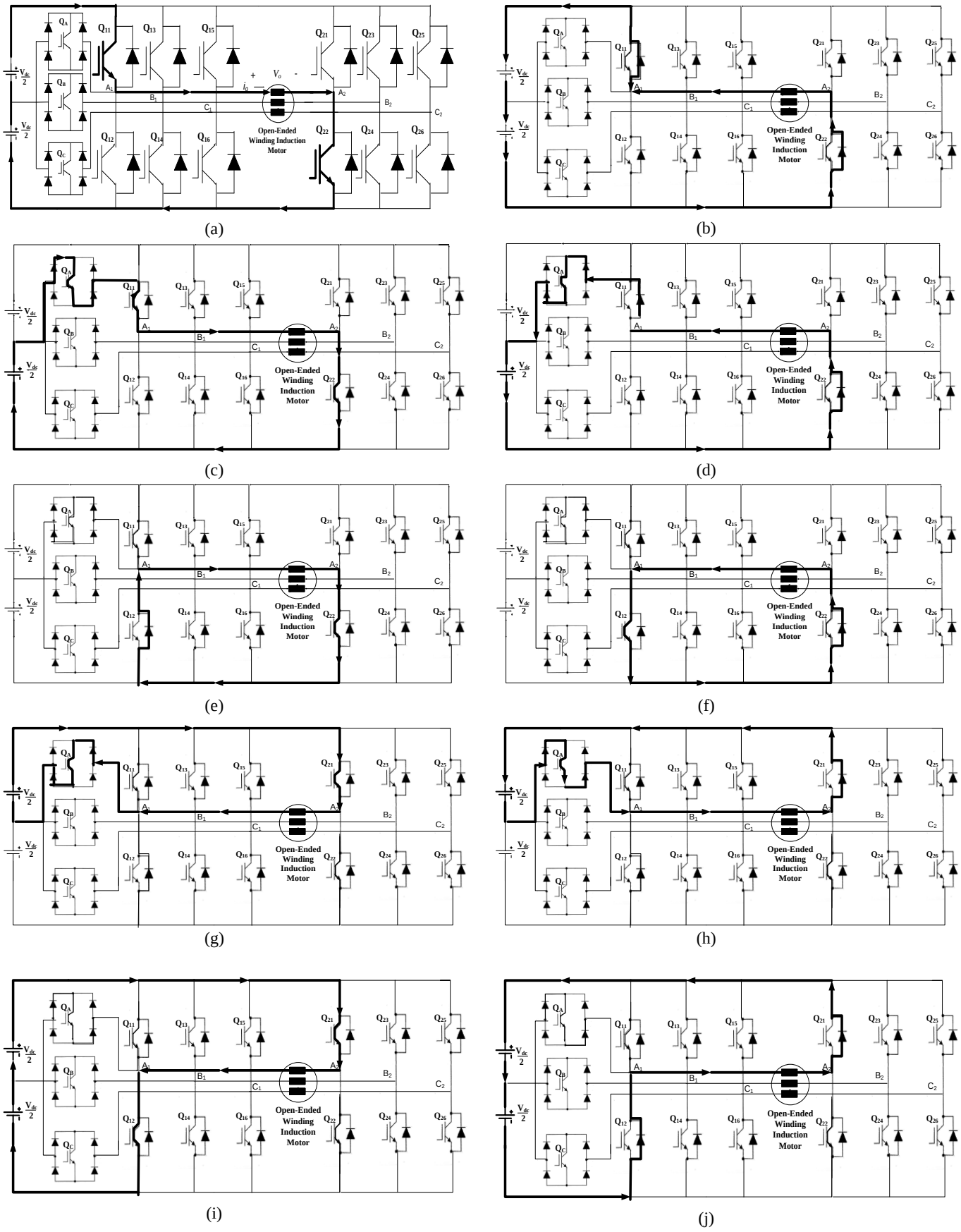

Fig. 2: Operation stages of phase A switches

3. MODULATION SCHEME FOR THE PROPOSEDINVERTER

During one cycle of the output the inverter operates through four modes. These operational modes are shown in Fig. 3 with respect to the per unit (PU) output voltage signal. Each of these operational modes has a high level and a low level as shown in Table II.

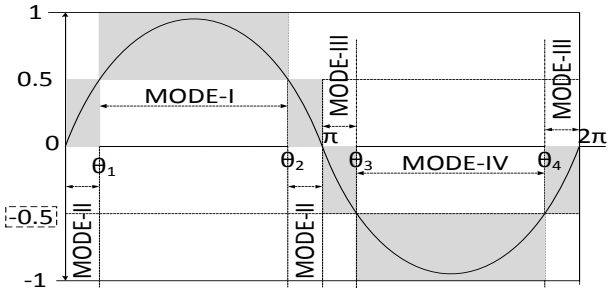

Fig. 3: Multilevel inverter switching modes with respect to the per unit (pu) amplitude of the output signal.

Basic principle of the proposed switching strategy is to generate gate signals by comparing the reference signal with the two carrier waves having same frequency and in phase, but different offset voltages [10, 26]. Three 120^o phase-shifted sinusoids are used as the reference waves for the proposed carrier-based sinusoidal pulse width modulation. The equations for the reference waves used in the proposed SPWM scheme for the present work are given by

$$V^*_{aref} = V_m \sin\omega t \quad (1)$$

$$V^*_{bref} = V_m \sin(\omega t - 120^0) \quad (2)$$

$$V^*_{cref} = V_m \sin(\omega t + 120^0) \quad (3)$$

Largely, there are two switching methods according to the output voltage levels. If the required output voltage for a certain load can be produced using half of the dc bus voltage, only the lower carrier wave is compared with the reference signal. The lower dc bus voltage is used to generate the output voltage. If the modulation index is equal or less than 0.5, the behavior of proposed inverter is similar to the three phase conventional full-bridge three-level PWM inverter. The method described above is the first operational mode.The phase angle depends on the modulation index, M_a index of the proposed five-level PWM inverter is defined as [26]

$$M_a = A_M / 2A_C \quad (8)$$

where A_C is the peak-to-peak value of carrier, and A_M the peak value of voltage reference V^*_{aref}. When the modulation index is less than 0.5, the phase angle displacement is equal to

$$\theta_1 = \theta_2 = \pi/2, \qquad \theta_3 = \theta_4 = 3\pi/2, \quad (9)$$

On the other hand, when the modulation index is greater than0.5, the phase angle displacement is determined by

$$\theta_1 = \sin^{-1}(A_C/A_M) \quad (10)$$

$$\theta_2 = \pi - \theta_1 \quad (11)$$

$$\theta_3 = \pi + \theta_1 \quad (12)$$

$$\theta_4 = 2\pi - \theta_1 \quad (13)$$

Fig. 4 shows the control signals generated by the signals C_{A1},$C_{A2}$and phase angle displacement (P_1-P_6). C_{A1},C_{A2} are outputs of comparators, which compare the respective carrier signals with the voltage reference V^*_{aref}, V^*_{bref} *and* V^*_{cref} i.e. if $V^*_{aref}$is less than top triangle then C_{A1} is 1 else it is 0, similarly if $V^*_{aref}$is less than bottom triangle then C_{A2} is 0 else it is 1. The gate signals ig_{11}, ig_{12}, ig_{21}, ig_{22} *and* ig_A of phase A, ig_{13}, ig_{14}, ig_{23}, ig_{24} *and* ig_B of phase B and ig_{15}, ig_{16}, ig_{25}, ig_{26} *and* ig_C of phase C are produced with the help the Boolean expressions which is implemented by the use of logical AND and OR gates. The switching functions of the proposed inverter for phase A are then given by following Boolean equation:

$$ig_{11} = \overline{C_{A1}} * P_2 + \overline{C_{A2}} * P_4 + \overline{C_{A2}} * P_6 \quad (14)$$

$$ig_{12} = \overline{C_{A2}} * P_2 + \overline{C_{A2}} * P_3 + \overline{C_{A1}} * P_5 \quad (15)$$

$$ig_{21} = P_4 + P_5 + P_6 \quad (16)$$

$$ig_{22} = P_1 + P_2 + P_3 \quad (17)$$

$$ig_A = C_2 * P_1 + C_{A1} * C_{A2} * P_2 + C_{A2} * P_3 + C_2 * P_4 + C_{A1} * C_{A2} * P_5 + C_{A2} * P_6 \quad (18)$$

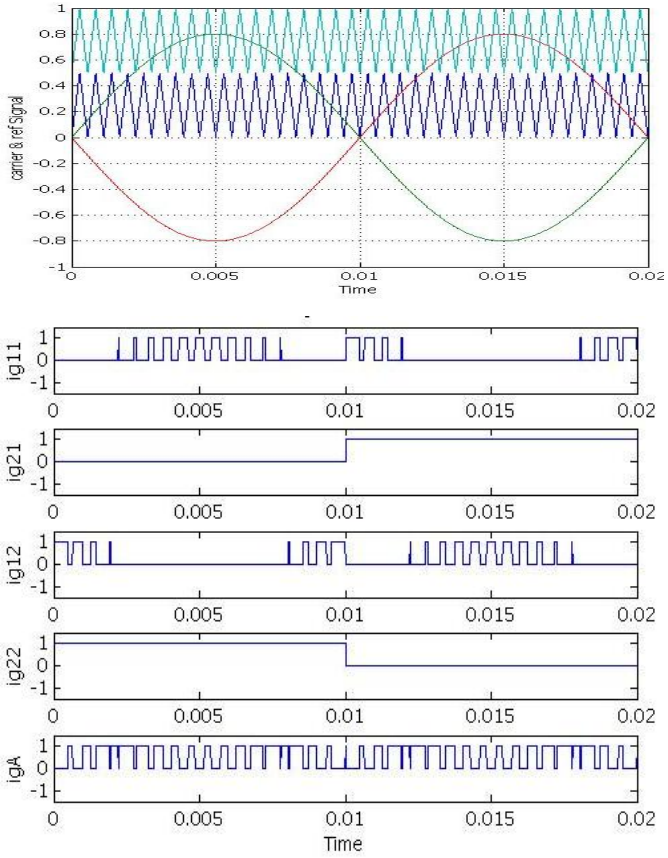

Fig. 4: Inverter switch gating signals using SPWM for phase A of the proposed inverter.

4. SIMULATION RESULT AND DISCUSSION

The performance of the proposed inverter has been observed on different type of loads like R, R-L in parallel, R-L in series, R-C in parallel and an open ended winding induction motor using MATLAB/SIMULINK. The simulation results have been shown in Figs. 5 to 8 for M_a of 0.8 and from Fig. 9 to Fig. 12 for modulation index M_a of 0.4 respectively. It is revealed that the inverter produces an output voltage that has a different number of levels depending upon the modulation index. The results presented in Fig. 7a-7c shows the phase

voltages V_{an}, V_{bn} and V_{cn} of the inverter for modulation index 0.8. Fig. 8a-8c shows the line voltages. Fig. 11a-11c and Fig. 12a-12c shows the phase and line voltages of the inverter for modulation index 0.4. Fig 13, 14, 16, 17 shows the R.M.S voltage, input power, output power, efficiency, power factor, R.M.S. current waveform for a 3 phase resistive load, series R-L, series R-C, parallel R-L respectively. The performance was observed for different load varying possibilities from 0-100% in steps of 25%. Fig. 15 depict a current THD of 1.17% for series R-L load. A closed loop PI controller was used in order to suppress the spikes developed in the voltages and current at the time of sudden change in the load. Fig 18 shows the stator phase A current, The performance of the proposed inverter driving a three phase open ended winding induction motor can be observed from Fig. 19 and Fig. 20 depicting R.M.S. output voltage, output power, input power, efficiency, power factor, R.M.S stator current and motor torque, speed and flux.

The performance of the proposed five-level PWM inverter is also compared with cascaded five-level PWM inverter reported in [15] and the comparison is listed in Table III. And Table IV. It is observed clearly from this comparison that not only the proposed inverter uses less number of switches and D.C sources, it gives higher fundamental voltage and lower voltage, current THDs also.

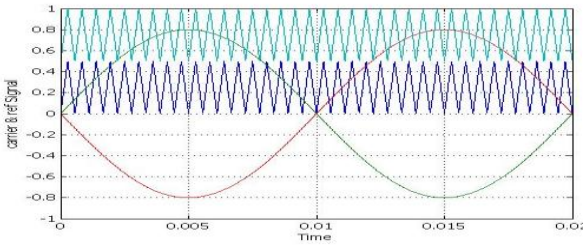

Fig. 5 The multicarrier PWM technique for M_a= 0.8.

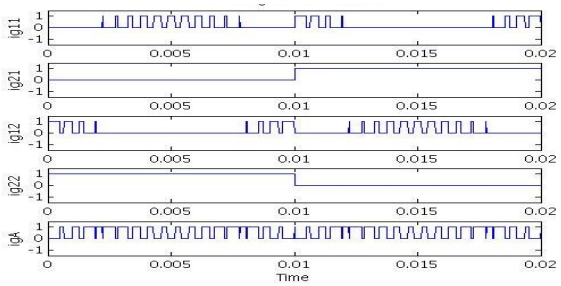

Fig. 6 Gate signals for Q_{11}, Q_{12}, Q_{21},Q_{22} *and* Q_A switches of phase A

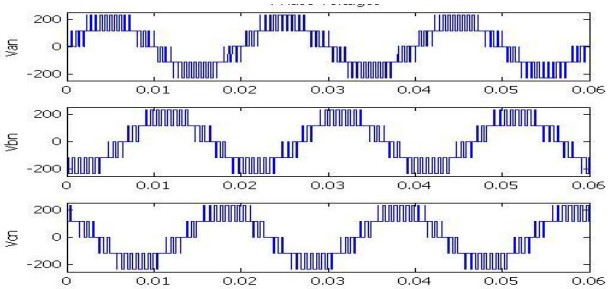

Fig. 7 Multilevel PWM inverter output phase voltages (van,vbn,vcn) for M_a= 0.8, M_f= 36, fs=50Hz.

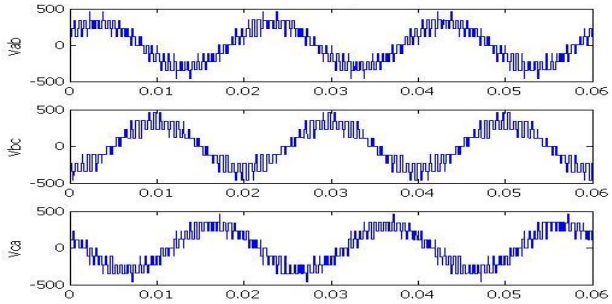

Fig. 8 Multilevel PWM inverter line voltages (v_{ab},v_{bc}, v_{ca})

M_a=0.8. M_f=36, f_s = 50Hz

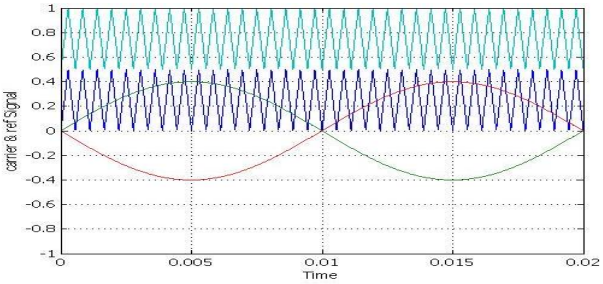

Fig. 9 The multicarrier PWM technique for M_a=0.4.

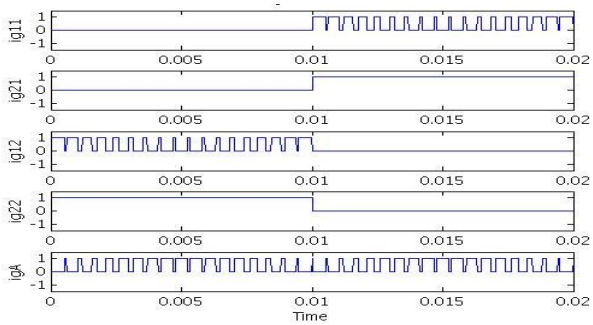

Fig. 10 Gate signals for Q_{11}, Q_{12}, Q_{21},Q_{22} *and* Q_A switches of phase A

TablE III
comparison of the cascaded inverter and the proposed inverter

	Conventional Cascaded Inverter [15]	Cascaded Inverter with open ended Induction motor[18]	Proposed Inverter with open ended Induction motor
Mainswitches	8	8	5
Main diodes	8	8	8
DC Sources	3	4	2

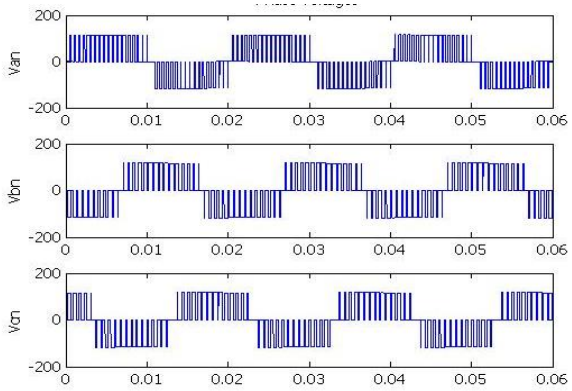

Fig.11 Induction motor Phase voltages for M_a=0.4, M_f=36, fs=50Hz

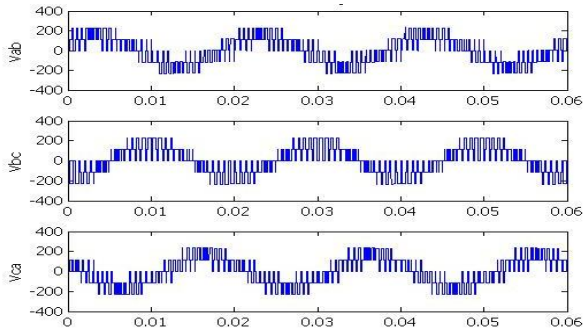

Fig.12 Line voltage for M_a=0.4, M_f=36, f_s=50Hz.

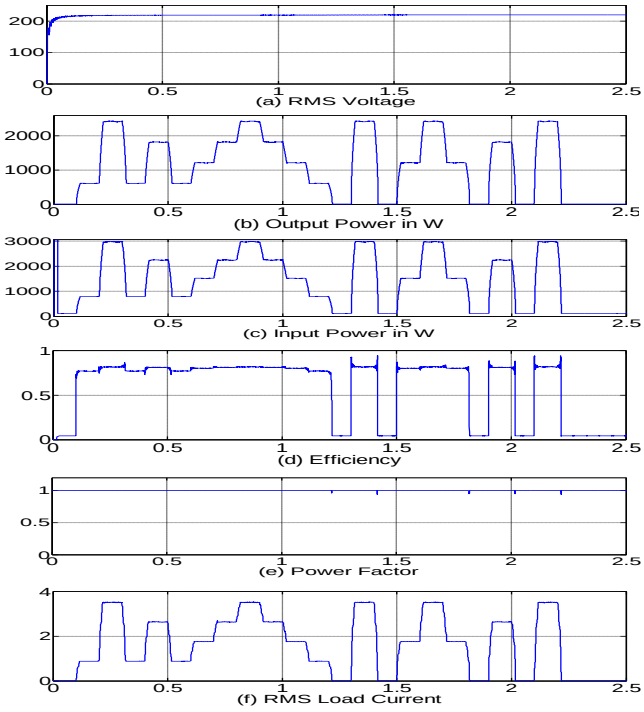

Fig.13 (a) R.M.S. Output voltage (b) Output power (c) Input power (d) Efficiency (e) Power factor (f) R.M.S. current of resistive load for different load variations M_a = 0.8, M_f = 36, f_s = 50Hz.

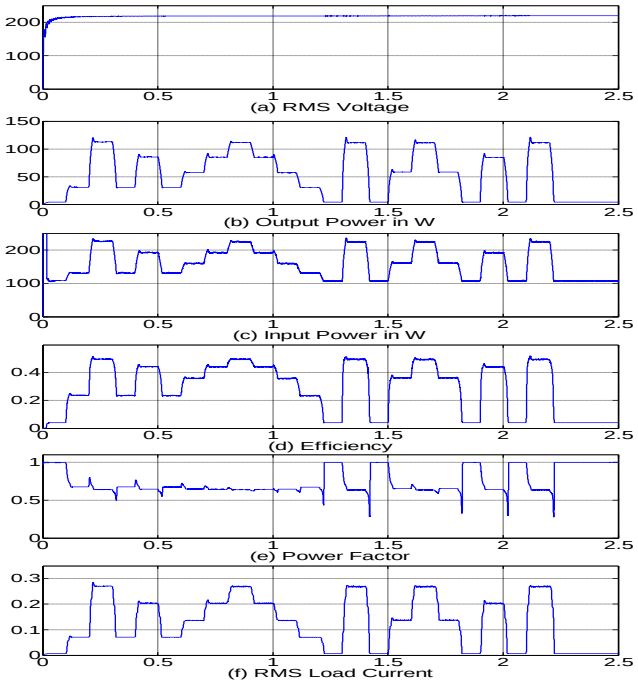

Fig 14(a) R.M.S. Output voltage (b) Output power (c) Input power (d) Efficiency (e) Power factor (f) R.M.S. current of R-L load connected in series for different load variations M_a = 0.8, M_f = 36, f_s = 50Hz..

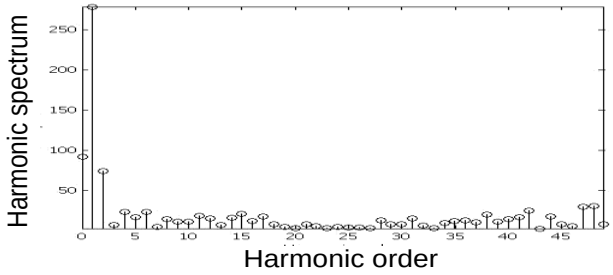

Fig. 15: The harmonic distortion spectrum , Current THD=1.17% for R-Lseries load

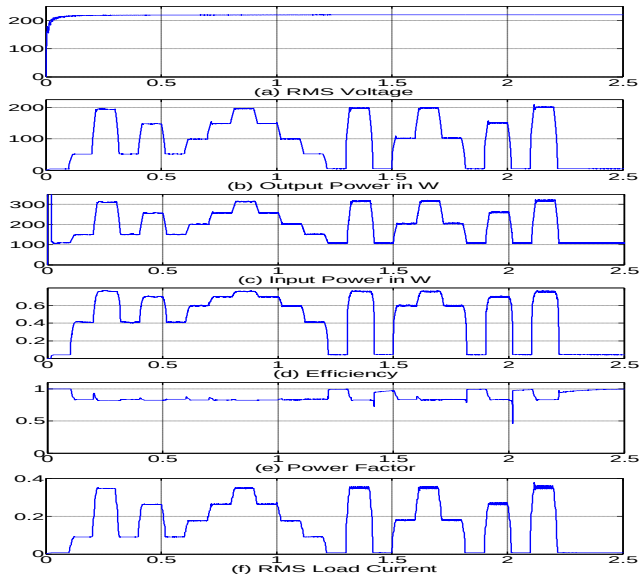

Fig 16: (a) R.M.S. Output voltage (b) Output power (c) Input power (d) Efficiency (e) Power factor (f) R.M.S. current of R-C load connected in series for different load variations M_a = 0.8, M_f = 36, f_s = 50Hz.

TABLE IV
comparison of the cascaded inverter [28] and the proposed inverter

Type of load	R load	R-L connected in parellel	R-C connected in parellel	R-L connected in series	Induction Motor
Fundamental voltage(V) [28]	165.1	166.4	167.2	166	165.4
Fundamental voltage (V) of proposed inverter	199.3	199.7	199.5	199.9	200
% Voltage THD [28]	37.61	37.64	37.62	37.91	38.1
% Voltage THD of proposed inverter	26.67	26.52	26.54	26.66	26.75
Fundamental current (A) [28]	1.909	1.27	1.204	1.214	9.471
Fundamental current (A) of proposed inverter	2.305	1.505	1.461	1.463	9.18
% Current THD [28]	37.6	28.4	53.37	1.99	8.62
% Current THD of proposed inverter	26.67	20.42	37.49	1.17	7.43

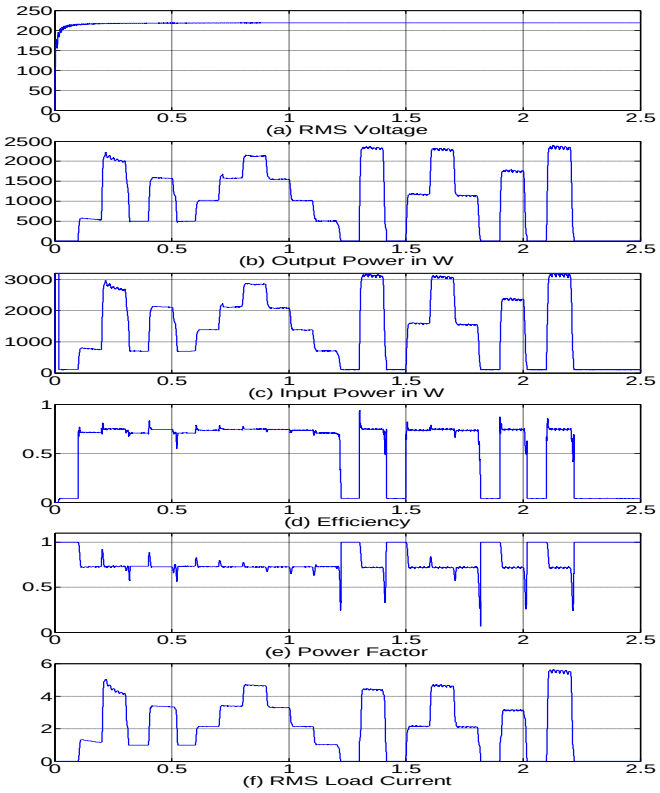

Fig 17: (a) R.M.S. Output voltage (b) Output power (c) Input power (d) Efficiency (e) Power factor (f) R.M.S. current of R-L load connected in parallel for different load variations M_a = 0.8, M_f = 36, f_s = 50Hz.

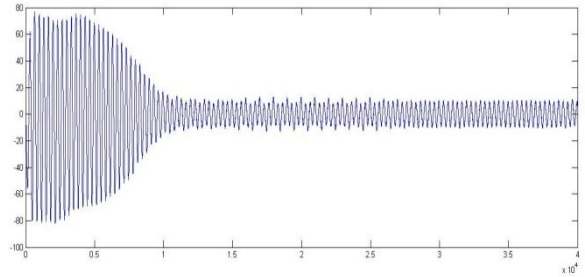

Fig 18: Stator current of phase A M_a = 0.8, M_f = 36, f_s =50Hz.

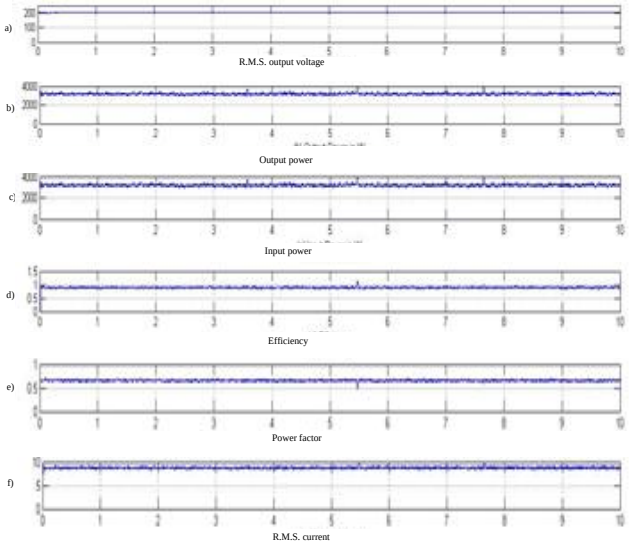

Fig 19: (a) R.M.S. Voltage (b) Output Power (c) Input Power (d) Efficiency (e) Power Factor (f) R.M.S. Current of Induction motor & M_a= 0.8, M_f = 36, f_s=50Hz.

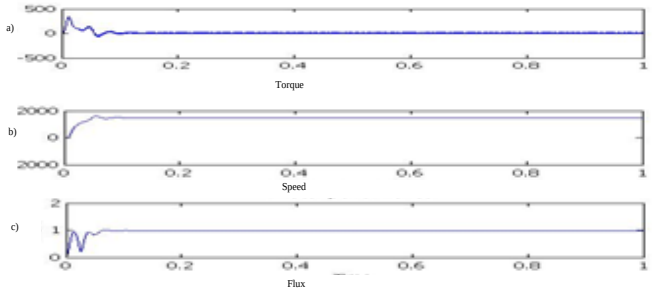

Fig. 20: Induction motor performance

5. CONCLUSION

The principle of operation of five level PWM three phase inverter for open ended induction motor has been presented in this paper. The proposed inverter consist of two, 2 level three phase inverter and three auxiliary circuit where, each auxiliary circuit has one switch and four diodes . The inverter generates a 5-level output waveform for modulation indexes above 0.5 and a 3-level output waveform for modulation indexes below 0.5. When compared with other five level inverters the proposed inverter uses less number of switches with improved performance. The power quality of the proposed inverter is better than that of conventional inverter [28] for different types of load.

6. REFERENCES

[1] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. IEEE PESC'98*, Cambridge, MA, 1998,pp. 96–103.

[2] P. M. Bhagwat*et al.*, "Generalized structure of a multilevel PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. 19, pp. 1057–1069, Nov./Dec.1983

[3] G. S. Buja, "Optimum waveforms in PWM inverters," *IEEE Trans. Ind.Applicat.*, vol. IA-16, p. 830, Nov./Dec. 1980.

[4] G. B. Kliman, A.B.Plunkett, "Development of a modulation strategy for a PWM inverter drive," *IEEE Trans. Ind. Applicat.*, vol. IA-15, pp. 72–79, Jan./Feb. 1979.

[5] M. A. Boost and P. D. Ziogas, "Toward a zero-output impedance UPS system," *IEEE Trans. Ind. Applicat.*, vol. 25, pp. 408–418, May/June 1989.

[6] T. Kawabata, T. Miyashita, and Y. Yamamoto, "Dead-beat control of three phase PWM inverter," *IEEE Trans. Power Electron.*, vol. 5, Jan. 1990.

[7] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[8] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[9] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2197–2206, 2010.

[10] V. G. Agelidis, D. M. Baker,W. B. Lawrance, and C. V. Nayar, "A multilevel PWM inverter topology for photovoltaic applications," in *Proc.IEEE ISIE'97*, Guimaraes, Portugal, 1997, pp. 589–594.

[11] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu- Rub," Model predictive control of multilevel cascaded H-bridge inverters," IEEE Trans. on Industrial Electronics, vol. 57, no. 8, pp. 2691–2699, 2010.

[12] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one DC supply," IEEE Trans. on Vehicular Technology, vol. 59, no. 8, pp. 3736–3743, 2010.

[13] T. Zumwalt, "DSP applications in the control of uninterruptible power supplies," in *Proc. ICSPAT'93 Conf.*, 1993, pp. 967–972.

[14] M. Calais, L. J. Borle, and V. G. Agelidis, "Analysis of multicarrier PWM methods for a single-phase five level inverter," in *Proc. IEEE PESC'01*, Vancouver, BC, Canada, 2001, pp. 1351–1356.

[15] Manjrekar, M.D., and Lipo, T.A.: 'A hybrid multilevel inverter topology for drive applications'. Proc. 13th IEEE Conf. on Applied power electronics (APEC), California, Feb 1998, pp. 523–529.

[16] Menzies, R.W., Steimer, P., and Steinke, J.K.: 'Five-level GTO inverters for large induction motor drives'. Proc. IEEE Ind. Appl.Soc. Annual Meeting, Toronto, 2–8 October 1993, pp. 595–601.

[17] Shivakumar, E.G., Gopakumar, K., and Ranganathan, V.T.:'Space vector PWM control of dual inverter-fed open-end winding induction motor drive', EPE J., 2002, 12, (1), pp. 9–18.

[18] M.R. Baiju, K. Gopakumar, K.K. Mohapatra, V.T. Somasekhar and L. Umanand, "Five-level inverter voltage-space phasor generation for an open-end winding induction motor drive",*IEE Proc.-Electr. Power Appl.*, Vol. 150, No. 5, September 2003.

[19] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi, "A reduced- switch-count five-level inverter with common-mode voltage elimina- tion for an open-end winding induction motor drive," IEEE Trans. Ind. Electron., vol. 54, no. 4, pp. 2344–2351, Aug. 2007.

[20] V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K. Mohapatra, and L. Umanand, "A multilevel inverter system for an induction motor with open-end windings," IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 824–836, Jun. 2005.

[21] K. Sivakumar, Anandarup Das, RijilRamchand, Chintan Patel, and K. Gopakumar, "A hybrid multilevel inverter topology for an open-end winding induction-motor drive using two-level inverters in series with a capacitor-fed H-bridge cell," IEEE Trans. Ind. Electron., vol. 57, no. 11, pp. 3707–3714, Nov. 2010.

[22] P. P. Rajeevan, K. Sivakumar, Chintan Patel, RijilRamchand, and K. Gopakumar, "A seven-level inverter topology for induction motor drive using two-level inverters and floating capacitor fed h-bridges," *IEEE Trans.Power Electron.*, vol. 26, no. 6, pp. 1733–1740, Jun. 2011.

[23] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimina- tion and DC-link capacitor voltage balancing using only the switching-state redundancy—Part I," IEEE Trans. Ind. Electron., vol. 54, no. 5, pp. 2600–2608, Oct. 2007.

[24] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "A dual five-level inverter-fed induction motor drive with common-mode voltage elimina- tion and dc-link capacitor voltage balancing using only the switching-state redundancy—Part II," IEEE Trans. Ind. Electron., vol. 54, no. 5, pp. 2609–2617, Oct. 2007.

[25] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[26] S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single-phase five level PWM inverter employing a deadbeat control scheme," *IEEE Trans.Power Electron.*, vol. 18, no. 18, pp. 831–843, May 2003.

[27] Zhong Du, Member, Leon M. Tolbert, BurakOzpineci, and John N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded h-bridge multilevel inverter," *IEEE Trans.Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan. 2009.

[28] P. Giroux and G. Sybille, "power_3phPWM3level.mdl" SIMULINK *demos* of MATLAB R2011A, version 7.12.