A Comparative Study on the Power Delay Product of Efficient Adders

International Journal of Computer Applications
Foundation of Computer Science (FCS), NY, USA

Volume 163
Number 3
Year of Publication: 2017

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10.5120/ijca2017913491

Abstract

In realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. There exists a trade-off between the design parameters such as speed, power consumption, and area. Adders are the most comprehensively used components in many circuits and they are building block arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its execution and power optimization is of at most importance. This paper proposes design of fast adders using two new dynamic logics named D3L (Data Driven Dynamic Logic) and sp-D3L (split pre-charge – Data Driven Dynamic Logic). Examination of two circuits, D3I and SP-D3L are made by using the software, Cadence Virtuoso. Power Delay Product (PDP) is calculated for both these logics.

References
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Index Terms

Computer Science Circuits and Systems

Keywords

Data Driven Dynamic logic, Split path Data Driven Dynamic, pull-up network (PUN), pull- down network (PDN), Power delay product.