A Comparative Study on the Power Delay Product of Efficient Adders

Anjana Jain Tom
Electronics and communication
Saintgits College of Engineering,
Kottayam,
Kerala, India

Remya Susan John
Electronics and communication
Saintgits College of Engineering,
Kottayam, Kerala, India

Sanjana Accamma Kurian
Electronics and communication
Saintgits College of Engineering, Kottayam,
Kerala, India

Susan Jose
Electronics and communication
Saintgits College of Engineering, Kottayam,
Kerala, India

Ashly John
Electronics and communication
Saintgits College of Engineering, Kottayam,
Kerala, India

ABSTRACT
In realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high- speed are the two predominant factors which need to be considered. There exists a trade-off between the design parameters such as speed, power consumption, and area. Adders are the most comprehensively used components in many circuits and they are building block arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its execution and power optimization is of at most importance. This paper proposes design of fast adders using two new dynamic logics named D3L (Data Driven Dynamic Logic) and sp-D3L (split pre-charge – Data Driven Dynamic Logic). Examination of two circuits, D3l and SP-D3L are made by using the software, Cadence Virtuoso. Power Delay Product (PDP) is calculated for both these logics.

General Terms
Dynamic logic, Efficient adders, VLSI, Data path sub-systems, Performance analysis, FPGA.

Keywords
Data Driven Dynamic logic, Split path Data Driven Dynamic, pull-up network (PUN), pull- down network (PDN),Power delay product.

1. INTRODUCTION
Addition forms the basis for many processing operations, from counting to multiplication to filtering. As a result, adder circuits are of great interest to digital system designers. Most high performance circuits, both general purpose processors as well as application specific architectures employ several arithmetic circuits. Since arithmetic circuits often form the critical components in a data path sub-system, the overall performance and throughput of these systems depends on the speed and power efficiency of the critical arithmetic components [3]. In all digital circuits, delay, power and area have since long been the primary considerations in full- adder design.

Various solutions have been proposed at the circuit level to achieve the optimum trade-off between delay, power and area in adder cells. Over the years, several new adder designs have been proposed to achieve optimum performance, power and area [2]. Besides these, several interesting combinations of logic and circuit design have been proposed to optimize full adder circuits. The new dynamic logic family, named Data Driven Dynamic (D3L) Logic and Split - Path Data - Driven (SPD3L) Logic are introduced to design efficient adders.

2. PRESENT LOGICS

2.1 CMOS Static Logic
CMOS static gates implement logic functions exploiting two complementary networks: the pull-up network (PUN) and the pull-down network (PDN), composed of, respectively, PMOS and NMOS transistors. There are two main limitations on the speed performances, especially for high fan-in gates: the large input capacitance and the contention between the PUN and the PDN during the gate switching. In order to counteract these drawbacks, dynamic domino logic is typically preferred for the design of high-speed data paths.

2.2 Dynamic Domino Logic
Standard CMOS Dynamic Domino circuits work utilizing a grouping of pre-charge and examination stages engineered by the framework clock hail. During the pre-charge phase, the output signal is forced to a pre-defined value on the other hand, during the evaluation phase; the output signal can change depending on the input signals. Fast and low locale inheritance makes dynamic domino the most by and large used method of reasoning in predominant microchips

In dynamic domino gates, the PDN (PUN) implements the logic function (evaluation network), while the PUN (PDN) is replaced by a single PMOS (NMOS) which is driven by the global clock signal [3]. Unfortunately, the clock distribution network dissipates from 20 to 45% of the overall consumed power, thus preventing the use of dynamic domino circuits in low-power applications. Moreover, the distribution of the clock signal involves non-trivial design issues, such as controlling skew and jitter.

Domino logics are speedier than their static CMOS accomplices in the meantime; of course, they are weaker to noise signal. This is a direct result of the spillage streams traveling through the PDN (PUN), which can achieve an undesirable discharging (charging) of the element nodes. To balance this impact, an input PMOS (NMOS) transistor is

exploited [3].However, the keeper has a negative effect on dynamic energy consumption and speed performances. In fact, during a switching of the gate, the keeper generates a DC contention with the PDN (PUN) causing short current energy dissipation. Moreover, the discharging or charging of the dynamic node is slowed, increasing the gate delay. The dynamic energy overhead and speed degradation are directly proportional to the width of the keeper [5]. The latter is sized in accordance with the number of the leakage paths within the PDN (PUN): the higher the leakage current flowing through the PDN (PUN) the wider the keeper to assure a reasonable noise tolerance.

3. DATA DRIVEN DYNAMIC LOGIC

In order to reduce the power consumption of dynamic circuits, data-driven dynamic logic (D3L) is proposed**.** The clocked pre-charging transistor is replaced by a data-driven pre-charge network that allows the clock distribution network to be completely eliminated and the power consumption to be significantly reduced [4]. The proposed adder circuit provides the speed advantages of dynamic design styles without the additional power consumption associated with the design of the clock distribution network, to provide excellent performance metrics in terms of speed, area, power, reliability and driving strength.

3.1 Carry Circuit

The design of the PDN is done by carefully selecting a combination of inputs such that the discharge path to ground is completely cut-off during the pre-charge phase.

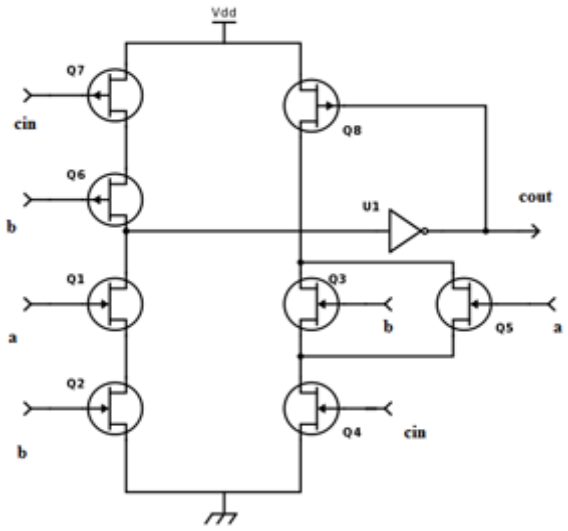

Fig 2: Full Adder Implementation in SP- Data Driven Dynamic Logic – COUT

The full adder circuit to find CARRY using pure D3L design methodology is shown in Figure 3.

3.2 Sum Circuit

As per conventional D3L logic methodology, the design of the PDN is done by carefully selecting a combination of inputs such that the discharge path to ground is completely cut-off during the pre-charge phase. As a general rule, the critical transistor combinations closest to the supply and ground rails are designed to be duals of each other [6]. This means, a parallel combination of three NMOS transistors driven by A, B, C which connects to the ground rail, is dueled by a series connection of PMOS transistors driven by the same signals. The remainder part of the logic path in the PDN does not need to be copied in the PUN.

A full adder circuit to find SUM using pure D3L design methodology is shown in Figure 2.

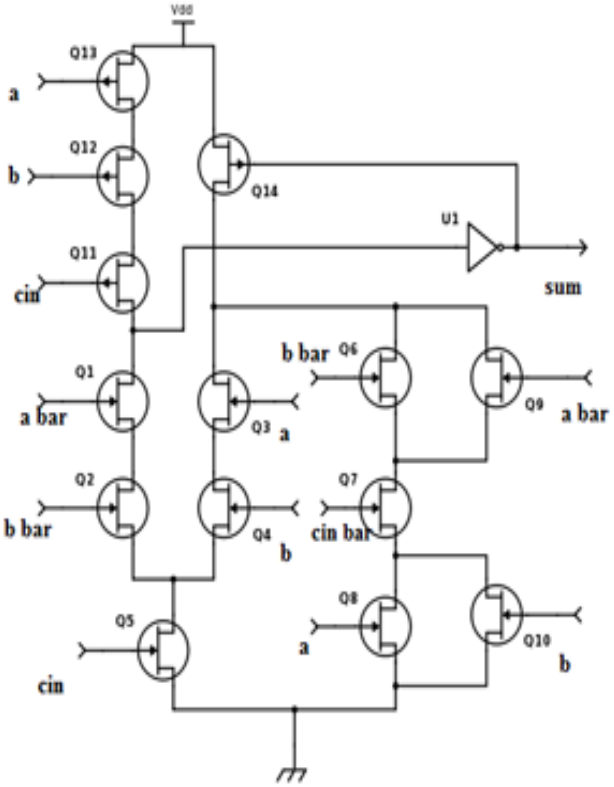

Fig 3: Full Adder Implementation in Conventional Data Driven Dynamic Logic – SUM

4. SPLIT - PATH D3L

Although the arrangement of D3L offers advantages over other dynamic styles, it suffers from longer pre-charge times and poor fan-in, due to the series stacked PMOS transistors. We observed that it is possible to improve the performance of the adder design by reducing the capacitance at the output node. This allows for higher fan-in, lower pre-charge times and relaxed sizing requirements [4]. The new adder design with reduced pre-charge capacitance is Split Path – Data Driven Dynamic Logic.

A first perception after taking a gander at any full adder design is the generally little and simple CARRY path contrasted with the SUM circuit. Because of the generally simple logic function and less transistors, the CARRY path utilizes lesser number of internal nodes. The capacitance at the output node is reduced due to smaller size of devices [7]. The pre-charge time and the probability of charge sharing are also reduced as a result of it. Thus, the circuit is generally less defenseless to speed and signal integrity troubles. To get a better sum path, in this way it is logical to consolidate some of these factors in the design of the pull-up and pull-down networks.

To enhance the slow pre-charge stage of the SUM path in the original D3L adder, we here, split the pre-charge path into

two. We also divide the design of the PDN into two paths. Viably, the output node from the first D3L logic has now been part into two, marked by D1 and D2. This splitting results in significantly reduced capacitance at the output node of our new circuit.

The circuit likewise accomplishes a level of resistance to charge-sharing issues, by combining with faster pre-charge. This approach of split-path effectively divides equally the conceivable paths for charge sharing within the adder circuit, when contrasted with the conventional D3L or standard domino designs [2]. The signals from D1 and D2 drive a standard CMOS NAND structure to create the final output. A SUM output which is inverted, goes back to drive the gates of the two keeper transistors. Thus, we can restore the charge on D1 and D2 through a common path, allowing the two nodes to restore simultaneously. This minimizes the probability of any incorrect operation.

The SP-D3L adder circuit in this manner incorporates the key favorable factors of D3L logic style and that of the standard CMOS. By using a shorter pre-charge path, we get a faster circuit operation. We get a large noise margin, improved signal robustness, sharper rise and fall times as well as an overall increase in reliability, from the final standard CMOS topology [6]. Splitting leads to lesser number of stacked PMOS and NMOS transistors. It results in relaxed sizing of the transistors and translates into an improved fan-in and fan-out performance of the circuit in both super-threshold and sub-threshold operating regions.

The SUM has been split into two functions D1 and D2. This is to split the pre-charge path in the conventional D3L. The SUM is finally obtained by the NAND of D1 and D2. If we consider any dynamic implementation, we can see that the pre-charged node loses charge either when the function evaluates to zero or when there is charge leakage, charge sharing, and, capacitive coupling. Therefore, in dynamic circuits, to maintain correct pre-charge at this node, keeper transistors are usually used as pre-charge or pre-discharge transistors. In the implementation of SUM, the signals D1 and D2 drive these keeper transistors. This ensures that whenever the SUM output evaluates to 1, either of the two nodes D1 and D2 are discharged to ground, the keepers driven by signal OUT, thus helping in restoring the charge during the pre-charge phase.

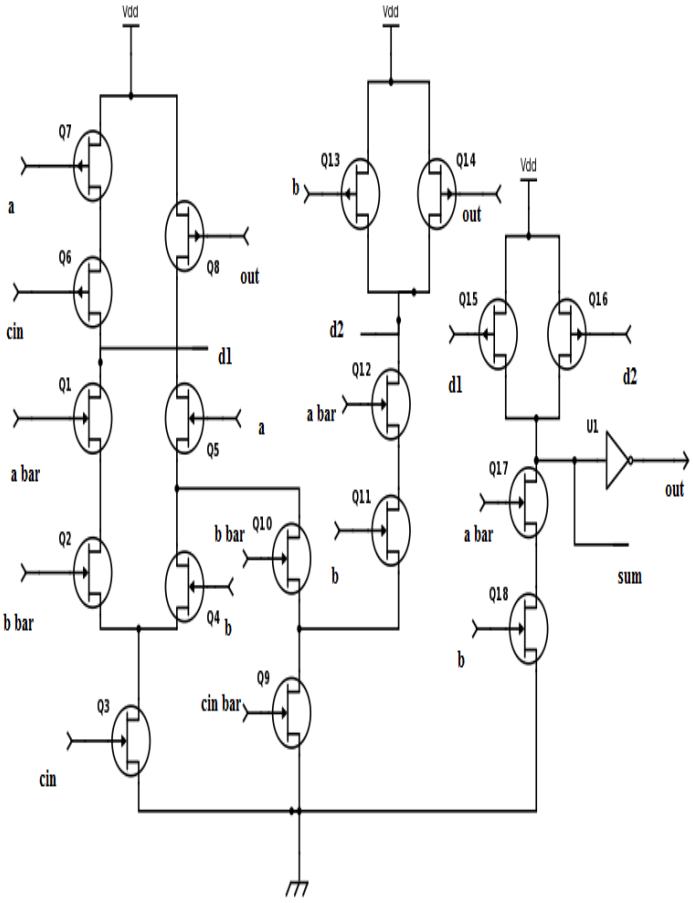

Fig 4: Full Adder Implementation in SP- Data Driven Dynamic Logic – SUM

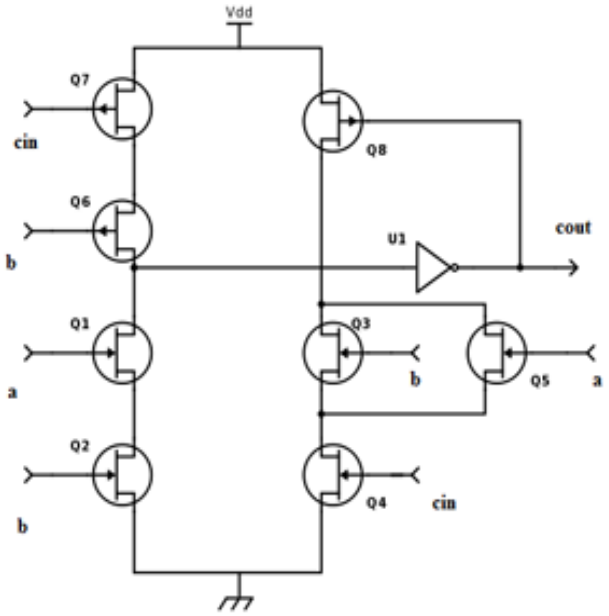

Fig 5: Full Adder Implementation in SP- Data Driven Dynamic Logic – COUT

5. ANALYSIS AND RESULTS

The examination which consolidates the two circuits, D3L and sp-D3L, been established on propagation continues running on Cadence Virtuoso 6.1.6.The supply voltage is 3.3V. By enhancing the transistor sizes of full adders considered it, is possible to decrease their deferral without on a very basic level growing the power use, and transistor sizes can be set to achieve slightest PDP.

The table below shows the performance comparison of the D3L and SP-D3L adders.

Table 1. Comparison of Adders

LOGIC	Rising to Falling (s)	Falling to Rising (s)	Average delay(s)	Power (mV)
D3L				
COUT	5.08n	-4.954n	5.006n	1.01
SUM	5.119n	-4.952n	5.0355n	1.89
SP-D3L				
COUT	5.08ns	-4.954n	5.006n	1.01
SUM	0.193ns	-4.927n	2.56n	1.07

Calculation of Power delay product utilized by D3L is 14.613pWs and SP-D3L is 7.786pWs. From above analysis it is clear that power delay product is less for SP-D3L logic thus SP-D3L is superior logic.

Fig 6: PDP Comparison of D3L and SP – D3L

From the analysis, it is clear that the PDP of SP-D3L is just half of D3L.

6. CONCLUSION

The quantitative overview of performance of the full adder cell using D3L and SP-D3L has been presented. The investigation which includes the four circuits SUM and carry of these two logics has been based on simulation runs on Cadence Virtuoso environment.

The new split-path implementation of the full adder function was observed to be a solid contender as far as both performance-power efficiency as well as strong driving capability. From the perspective of unwavering quality and robustness, to process variations, these adders are required to fare better than ordinary dynamic domino adders.

The PDP is the quantitative measure of the efficiency of the trade-off between power dissipation and the speed, and is particularly important when low power operation is needed. Hence, SPD3L can be thought to be more productive than D3L.

7. ACKNOWLEDGMENTS

We would like to acknowledge the Department of Electronics and Communication, Saintgits College of Engineering, Kottayam for the technical support in simulations.

8. REFERENCES

[1] Sohan Purohit, Marco, and Martin Margala, "Design Space Exploration of Split-Path Driven Dynamic Full Adder", Journal of Low Power Electronics Vol.6,1-13,2010.

[2] G.Karthik Reddy, D.Sharat Babu Rao, "A Comparative study on Low-Power and High Speed Carry Select Adder", IEEE Sponsored 9th International Conference on Intelligent Systems and Control (ISCO) 2015.

[3] Ms Anagha U P, Mr. Pramod P, Power and Area Efficient Carry Select Adder, IEEE Recent Advances in Intelligent Computational Systems(RAICS) , Dec 2015

[4] Sohan Purohit, Martin Margala, "Investigating the Impact of Logic and Circuit Implementation on Full Adder Performance", IEEE transactions on Very Large Scale Integration (VLSI) Systems, Vol 20. No. 7, July 2012.

[5] Vivek Kumar, Vrinda Gupta and Rohit Mayura, "A Study and Analysis of High Speed Adder in Power Constrained Environment", International Journal of Soft Computing and Engineering (IJSCE) , ISSN: 2231-2307 Vol 2,Issue -3, July2012

[6] A. Shams, T. Darwish, and M. Bayoumi, "Performance analysis Of low power 1-bit CMOS full-adder cells",. IEEE Transactions on VeryLarge Scale Integration (VLSI) Systems 10, 20 (2002).

[7] Rafati R., Fakhraie S.M., Smith K C.: „A 16-bit barrel-shifterimplemented in data-driven dynamic logic (D3L)", IEEE Trans. Circuits Syst. I, 2006, 53, (10), pp. 2194–2202

[8] F. Frutaci, M. Lanuzza, P. Zicari S. Perri, P. Corsonello " Low Power Split Path Data Driven Dynamic Logic" published in IET Circuit Devices & Systems 20th April 2009.