Diode Switch: A Novel Technique for Mitigation of Leakage Power in DSM Technologies

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ABSTRACT
As technology scales down below 65nm there is a rapid growth in semiconductor industries; reduction in transistor size leads to exponential increase in power consumption in DSM technology. The major concerns of VLSI designers are to develop a circuit which is having high performance with minimal size earlier. The fast growth in portable computing and wireless communication has led to the power dissipation along with heating. In this paper we have implemented a novel leakage reduction technique known as Diode switch (Combination of PMOS and NMOS sleep transistor) and inserted a sleep transistor above PUN and below PDN which increases the resistance of the circuit. By inserting the sleep transistor short circuit power consumption reduces which rail the circuit from supply voltage, but there is penalty of area take place. All the simulation is performed 32nm technology by using HSPICE simulator. Proposed DHS circuit reduce 48.98%, DFS reduces 52.89% and DHFS reduces upto 68.27% of leakage power.

Keywords
Leakage Reduction, High speed, Low power, DSM

1. INTRODUCTION
As the in semiconductor industries progress by following Moore's law faithfully from last five decades, and integrating more transistors along with functional circuits on a single chip periodically with every coming process technology [1-3]. However, this progress help in rapid run towards tiny, circuit design high speed and economical VLSI (Very Large Scale of Integration) circuits has added to excessive power dissipation of numerous circuits used today. Power dissipation is a main attention in the design of CMOS VLSI circuits [4]. High power consumption in low power VLSI reduce the life of the battery in the case of portable battery operated device and which affects the reliability, packaging and cooling overheads of the current in nanoscale [4-6]. The major concerns of VLSI designers are to develop a circuit which is having high performance with minimal size earlier.

A number of techniques have already been proposed for reducing power dissipation. The two important types of power dissipation in VLSI circuits are 1) Static power dissipation and 2) Dynamic power dissipation. While static power dissipation is due to internal leakages in devices during the off state of a circuit [1], dynamic power dissipation is because of the energy loss during charging and discharging of the output node capacitance of a transistor when switching takes place. Lately, dynamic power dissipation has been the primary concern of designers. Different technologies have been introduced over the years which are sub-threshold logic [3]. This is the main concern for development of low power consumption circuit in DSM technology. While scaling of technology also reduces the supply voltage (Vdd) which reduces the switching activity of the transistor which is the main cause in IC for total power dissipation[7-9].

The organization of the paper is as follows: The section II, describes previous work which consist various types of leakage current and techniques to reduce the leakage current. Section III presents a proposed work of leakage reduction by Diode transistor. Section IV shows the result and Discussion of existing and proposed circuit by using HSPICE EDA Tool. Finally the conclusion is presented in section V.

2. PREVIOUS WORK
There are various types of Leakage current present in CMOS devices as we scale down the channel length some of the Leakage current present in CMOS as shown in Fig.1[5].

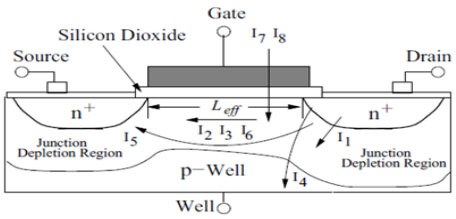


Fig.1. Leakage Mechanism in Short-Channel NMOS Transistor

I1= Reverse-bias p-n junction diode leakage current

I2 = Subthreshold leakage current

I3 = Gate Oxide tunneling current

I4 = Hot-carrier injection

I5 = Channel punch-through

I6 =Gate induced drain-leakage current

2.1 Leakage Power Reduction Technique
These is the leakage current dominant in CMOS circuit when channel length reduces below 180nm technology.

2.1 Sleep Mode Approach
In sleep approach addition PMOS transistor is inserted between pull up network and Vdd, NMOS transistor is inserted between pull down network and GND, sleep transistor turn off the circuit by cutting from the power supply, No direct path is form between Vdd to GND [2]. to discharge the supply voltage as shown in Fig.2. The sleep transistor turns off the circuit when it is in ideal mode, and turn ON the circuit is in active mode [10]. The sleep transistor cut from the power supply of main circuit, this technique reduces the leakage current efficiently. But there is problem arises of output Logic which is not achieve properly. Additional hardware used to provide sleep signal increases the area requirement of the circuit. During the standby mode these transistors are turned off and introduce large resistance in the conduction path so that leakage power is reduced in the circuit as shown in Fig.1[3]. During the standby

mode these transistors are turned off and introduce large resistance in the conduction path so that leakage power is reduced in the circuit [2,9].

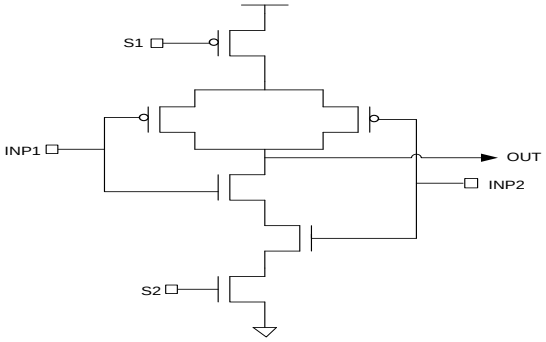


Fig.2. Sleep Approach NAND gate

2.2 Stack Approach

Another leakage power reduction technique is the stack approach, which forces a stack affect by breaking down an existing transistor into two half size transistors. Sub threshold leakage is exponentially related to the threshold voltage of the device, and the threshold voltage changes due to body effect [4]. From these two facts, one can reduce the sub threshold leakage in the device by stacking two or more transistors serially as shown in Fig.3 [5]. The transistors above the lowest transistor will experience a higher threshold voltage due to the difference in the voltage between the source and body as shown in Fig.3. However, forced stack devices have a strong performance degradation that must be taken into account when applying the technique [3-5].

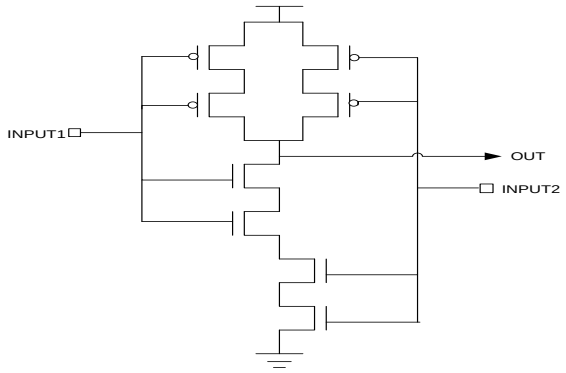


Fig 3: Stack Approach based 2 input NAND gate

2.3 Leakage Feedback Approach

Leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the output of the inverter is derived by the two transistors output of the circuit implemented utilizing leakage feedback [5-6].

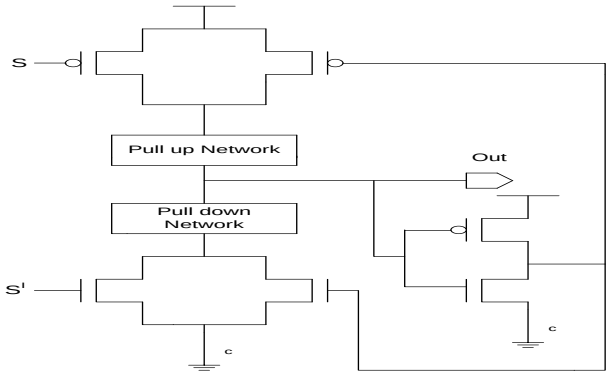


Fig.4. Leakage Feedback Approach

As shown in Fig.4. PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.

2.4 Sleepy Stack Approach

The main idea behind the sleepy stack technique is to combine the sleep transistor approach during active mode with the stack approach during sleep mode. The structure of the sleepy stack approach is shown in Fig. 5. In this approach we are dividing the existing [5] transistor into two transistors while maintaining W/L ratio of original transistor. We insert sleep transistors above pull up network and below pull down network parallel with stacked transistors; while divided transistors increases the resistance of the circuit which reduce the leakage power [5]. Sleepy stack technique is the combination of two well known techniques which divides existing transistors into two half without affecting the capacitance of the circuit. [6]. When circuit is in active mode, PMOS sleep transistor S=0 and NMOS sleep transistor S'=1 are asserted, at this stage all sleep transistors turned on. By added sleep transistor, the resistance of the activated (i.e., "on") path decreases, and propagation delay of the circuit also decreases (compared to not adding sleep transistors while leaving the rest of the circuitry the same, i.e., with stacked transistors First, leakage power is suppressed by high- transistors [4].

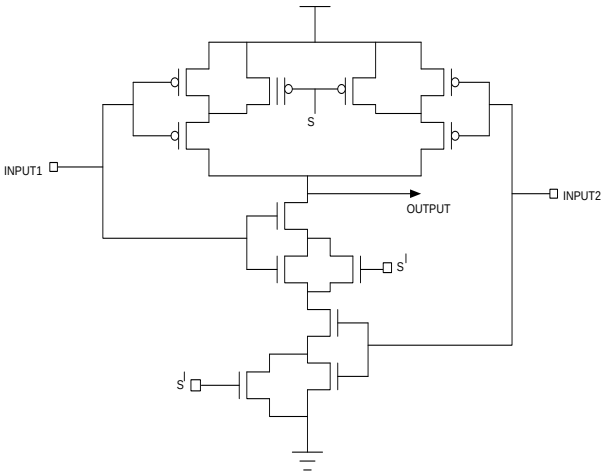


Fig.5. Sleepy Stack Approach based 2 input NAND gate

2.5 Sleepy Keeper Approach

Sleepy keeper is another approach of leakage power reduction in Deep submicron technology (DSM). The well know approach in which we insert PMOS sleep above pull up and VDD and NMOS sleep transistor is in between Pull down and GND to maintain the logic and reduces the leakage current of the circuit[9-12] to NMOS sleep transistor to maintain proper logic of the circuit we also known that PMOS transistors not efficient at passing GND; and NMOS transistors are not efficient at passing VDD. As shown in Fig. 6. When circuit enter in sleep mode, NMOS transistor only pass signal VDD to the pull-up network since the sleep transistor is off. For proper working of this approach NMOS transistor must be connected to VDD and the PMOS transistor should be connected to GND for maintain proper logic state of the circuit[7-8]. Sleep Keeper approach generate proper logic as shown in Fig.7.

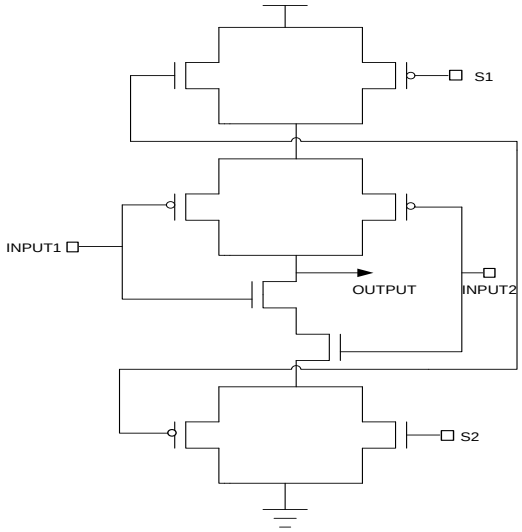


Fig.6. Sleepy keeper Approach based 2 input NAND gate

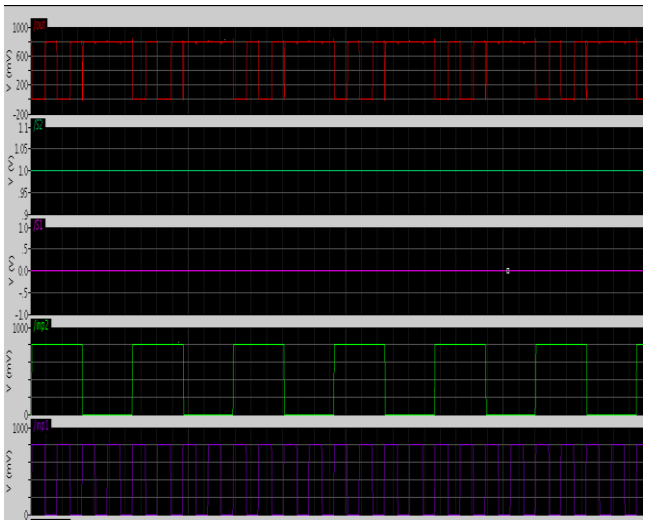


Fig.7. Output waveform of Sleepy Keeper approach with 2 input NAND gate

2.6 RBB Scaling with Technology

Body bias technique can be used in run time leakage current mitigation in this technique in this technique we apply reverse bias to the PMOS and NMOS transistor by increasing Vth of the transistor as shown in Fig.8. Body biasing is done by connecting reverse potential voltage between source and body terminal of the circuit. By applying a reverse body bias we increase the Vth of the transistor, the Vth is increase when source to substrate is of PN junction transistor is reverse bias this technique is called reverse bias technique [13-16]. While applying forward body bias the Vth of the transistor can be increase. In Fig.8, both PMOS and NMOS transistor are shown we apply reverse body biasing technique by applying –ve supply to both the transistor between source and substrate which reduces the leakage current. RBB is the runtime leakage reduction technique but it requires an addition controller circuit which can sense the optimum body potential for PMOS and NMOS circuit. Here extra DC supply is required [17]. Threshold voltage of PMOS and NMOS transistor is calculated in Table.I.

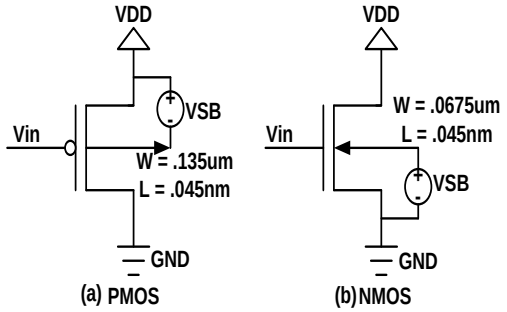


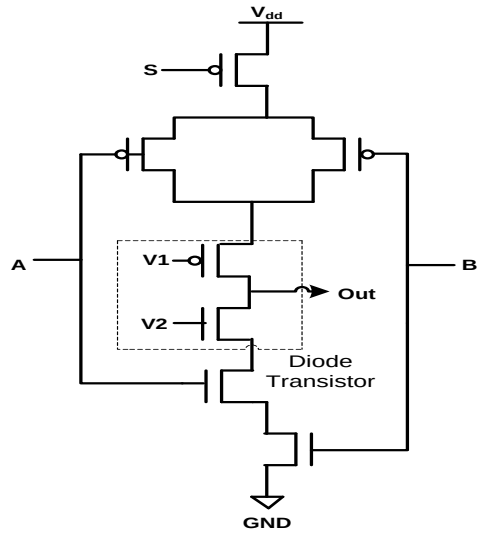
Fig.8: Calculation of Reverse body bias (a) PMOS and (b) NMOS transistor

Table 1. Threshold voltage of NMOS and PMOS

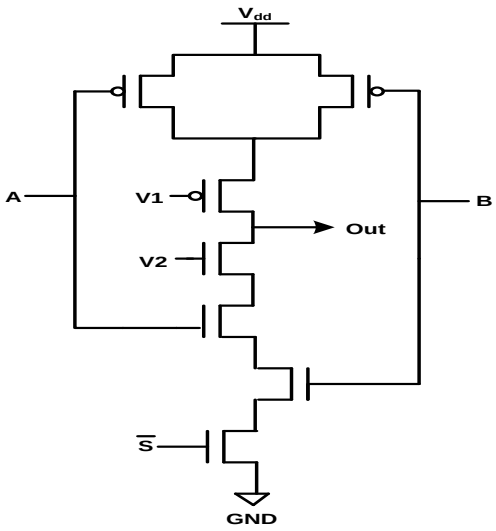
Threshold	Transistor voltage
NMOS Low V_{th}	-37mV
NMOS high V_{th}	345mV
PMOS low V_{th}	-83mV
PMOS high V_{th}	-393.9mV

3. PROPOSED WORK

In this section three new designees are introduced namely Diode Header Sleep (DHS), Diode Footer Sleep (DFS) and Diode Header Footer Sleep (DHFS), these are the combinations of self controlling and external leakage controlling technique as shown in Fig.9. In self controlling technique no external signals are applied while in external leakage controlling technique external sleep signal are applied which switches OFF the sleep transistor to reduces the leakage power. The basic idea behind all the proposed techniques is to provide stacking effect of the transistor which mitigates leakage power from Vdd to GND. To reduce the dynamic power in active mode both PMOS and NMOS sleep transistor turn ON and reduces the resistance of the circuit. To mitigate static power both PMOS and NMOS sleep transistor turn OFF provides the stacking effect and increase the resistance of the circuit which help in reduction of the leakage power. Circuit achieves proper logic because location of leakage controlled transistors is such a way that it passes good high logic and good low logic signal with small degradation of output voltage compared with LECTOR technique.



(a)



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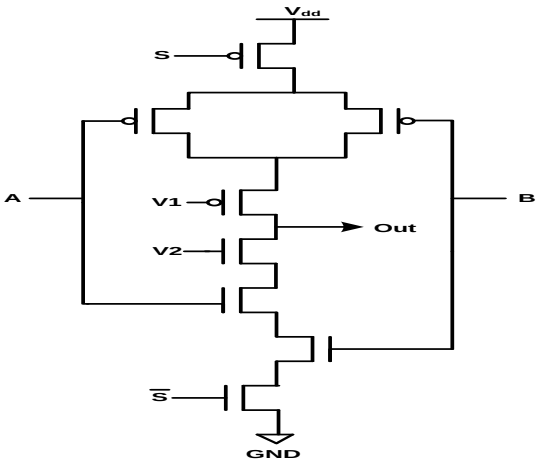
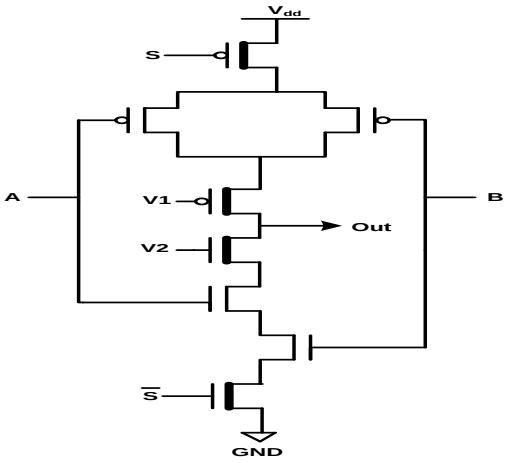


(c)



(d)

Fig.9 Proposed Circuit (a) DHS (b) DFS (c) DHFS (D) High Vth DHFS

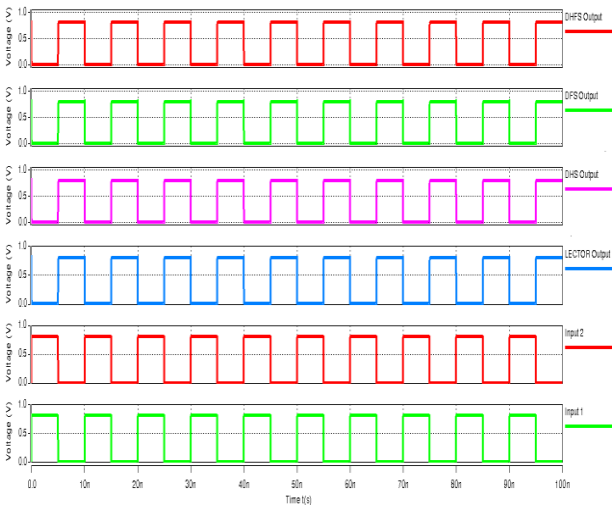


Fig.10: Transient characteristics waveform of 2-input proposed NAND gate using HSPICE in CMOS technology

Proposed DHS, DFS and DHFS is implemented for two input NAND gate. Proposed circuit reduces the leakage power by providing stacking effect with Diode technique and inserting of sleep transistor over pull up and pull down network which rail from Vdd to GND and increase the resistance of the circuit which help in reduction of the leakage power when circuit is in ideal mode. The output wave form of basic, existing and proposed circuit for two inputs NAND gate, here it can be seen that the LECTOR and proposed circuits does not achieve proper logic level because location of leakage controlled transistors is such a way that there is a small degradation of output voltage as shown in Fig.10.

4. RESULTS AND DISSCUSION

A 2 input NAND gate is simulated with leakage power reduction techniques sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS. After analyzing the results in terms of average power consumption, delay and PDP we conclude that sleepy stack with DTCMOS is producing comparatively better results. For calculation of switching power dissipation in MOS transistor we have to apply clock in the input show maximum switching activity take place for calculation of switching of the transistor a with the help of Transient Analysis all type of Average power dissipation and propagation delay of the given circuit is calculated. For

Calculation of transient response every test-bench circuit it is applied for the period on 20ns (as Transient Time), Average power, Dynamic Power, Delay is calculated in Table II.

For calculating transient response all circuit's schematics are designed on HSPICE Simulator in NOTPAD in .sp format and simulated it by using BISM simulation on Berkeley Predictive Model (BPTM) by using HSPICE 32nm process technology has been used for designing these circuits.

In this section the power dissipation of existing and proposed leakage reduction techniques is calculated. All the existing and proposed technique are simulated in HSPICE at 32nm CMOS technology with supply voltage of 0.8V, output capacitance CL =1pF, Leakage power is investigate at different temperature at 250C, The size (W/L) of all existing and proposed circuit made from P-MOS and N-MOS is same for fair comparison of results.

Process technology has been used for designing these circuits. Shows the results obtained for 2 input NAND gate with dual threshold transistors and reverse body bias and without reverse body bias in dynamic power calculation. The simulation results for 2 input NAND gate with sleep, forced stack, sleepy keeper and sleepy stack with DTCMOS and RBB are shown in the following Table III. in static power calculation for reduction of leakage power in nanosacle circuit design

Table 2: Average power, Dynamic power, Static power, Delay and PDP for 2 input NAND gate

32nm	Dynamic power (nW)	Static power (pW)	Delay (pSec)	PDP (1E-21)	EDP (1E-33)
Base	8.15	19.43	19.83	161.1	3194
Sleep	7.41	7.74	21.46	159.0	3412
Forced stack	7.68	9.34	26.84	206.1	5529
Sleepy keeper	7.54	8.05	29.74	224.2	6661
Sleepy stack	1.12	9.86	31.36	35.12	1101

Table 3. Percentage dynamic power saving for each Technique with RBB

32nm	Dynamic power(nW) With RBB	Dynamic power(nW) without RBB	Percentage saving (%)
Sleep	5.87	6.64	43.83
Forced stack	4.67	5.84	41.74
Sleepy keeper	6.82	7.24	49.57
Sleepy stack	7.48	9.84	57.84

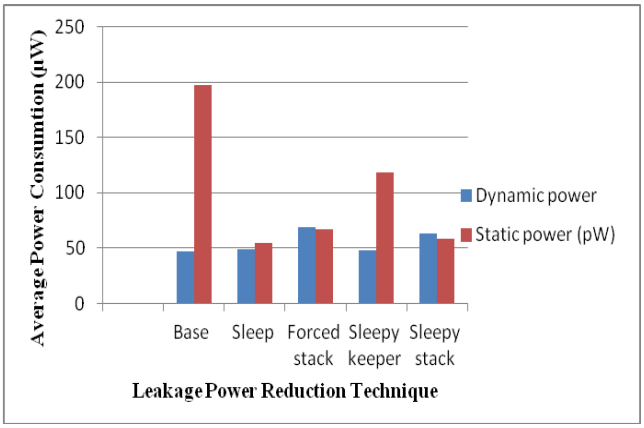


Fig 8: Comparison of Average Power consumption of sleep, forced stack, sleepy keeper and sleepy stack

A novel DHS, DFS and DHFS leakage reduction technique is proposed for low power application in digital circuits. Results show CMOS technology is used for ultra low power applications, reduction to design a device which is having lowest possible leakage. The experiment results shows that saving of dynamic power in proposed DHFS circuit is much lower than other circuits, the reduction is about 17.17% in NG, 25.68% in NGHS, 12.85% in NGFS, 25.75% in NGHFS and 2.86% in LECTOR, as shown in Fig.9. The proposed technique can be applied on high performance, low power applications, where leakage is major concern such as microprocessor, memory units and other portable devices.

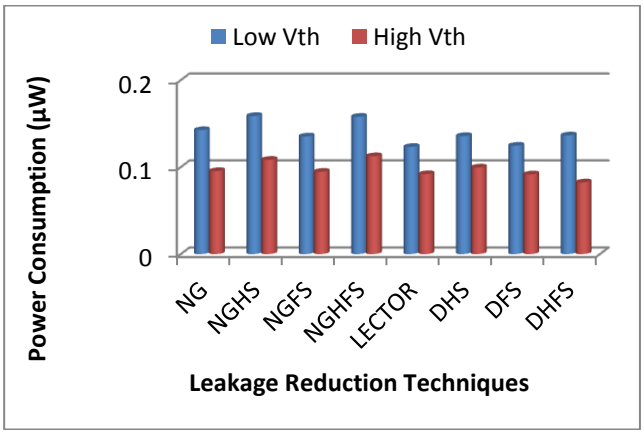
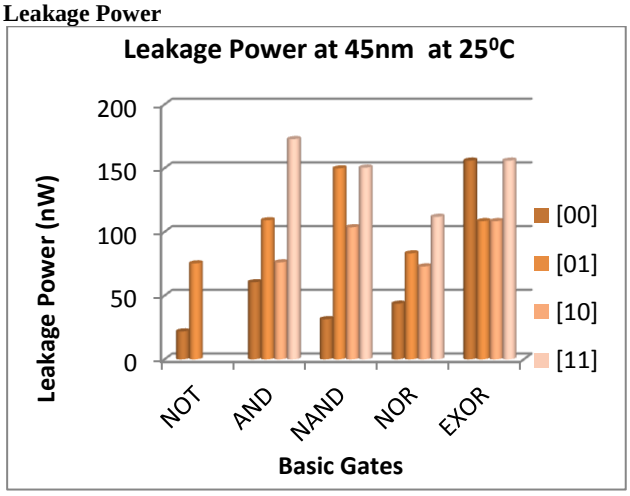
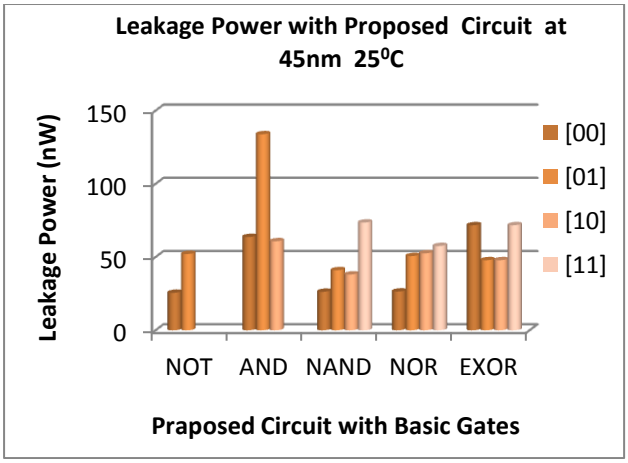
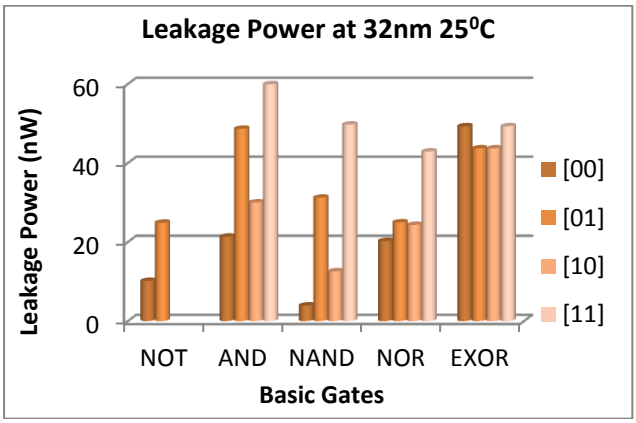


Fig. 9: Comparison of Average Power Consumption

Graphical Representation results for comparison of Leakage Power







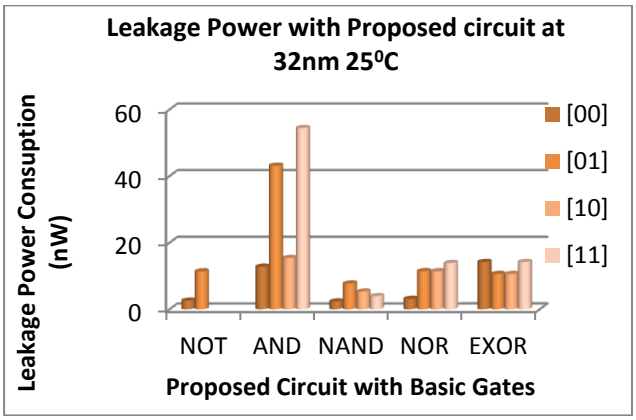


Fig.10: Results comparison between standard and proposed at various temperatures and various nanoscale design at 45nm and 32nm

5. CONCLUSION

In nanometer scale CMOS technology, subthreshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this technique a external controlling sleep transistor are inserted between PUN and PDN for increasing the resistance of the circuit, which help in mitigation of leakage power, we have tray all the combination by inserting Header and Footer Sleep transistor which rail the circuit to flow the current from VDD to GND. We have calculated the leakage current at 45nm and 32nm technology at 250C on all existing and proposed circuit for all input vector combination. Saving of leakage power in DHFS is 40.19% for Low Vth and 22.75% for High Vth, in DHFS 96.91% for Low Vth and 96.01% for High Vth at all input vectors as compared to LECTOR NAND gate. The proposed circuit shows better leakage reduction than existing techniques there is no requirement of additional power supply

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