Abstract

Double gate MOSFET technology is used wherever low power delay product is desired. It uses to reduce leakage current drain induced barrier lowering effect (DIBL) and other short channel affects. In this work 8×8, Booth Multiplier is analysed in 90nm technology, with one single-gate MOSFET technology and then other using the proposed that is Double-Gate MOSFET technique. Depending on the input patterns, the proposed technique saves 24% in power consumption has observed in proposed circuit. Design and simulations are performed in cadence virtuoso and spectre tools using 90nm technology.

References

16-Bit Multiplier based on Booth Algorithm”, International Journal of Advancements In Research and Technology, Volume1, Issue 6, November-2012 ISSN-2278-7763


Index Terms

Computer Science Circuits and Systems

Keywords

Booth Multiplier, Double Gate, Low power, Power Delay Product (PDP)