Abstract

The effects of aging of digital circuits are coming into focus due to observations made with several experiments and researchers have started working towards making changes for the improvements in base paper architecture. The integrated device suffers with NBTI and PBTI due to CMOS semiconductor properties and it affects the working of different logic operations and in the same context here we have taken multiplier for consideration and working to develop delay efficient multiplier with aging aware design using adaptive hold logic which is modified in this work to reduce effective delay to speedup circuit logic. The simulation of experiments are conducted in Xilinx IDE 13.1.

References


Index Terms

Computer Science  Circuits and Systems

Keywords
Adaptive hold logic, row bypassing, column bypassing, Multiplier, Aging Effect, NBTI, PBTI, Delay Efficient