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Design of a Three Stage Ring VCO in 0.18 µm CMOS under PVT Variations

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ABSTRACT
This paper describes the design of a 3.4 GHz three stage Ring Voltage Controlled Oscillator (VCO). In order to achieve wide tuning range at gega hertz frequencies a three stage ring oscillator based VCO is designed using differential delay cell. The linearity is achieved over a wide-tuning range from 1.5 GHz to 3.8 GHz while maintain the phase noise -116 dBc/Hz at 3.4GHz.The designed VCO is simulated using Cadence 0.18-µm CMOS process and VCO consumes 8.58 mA current and 15.4mW power from a 1.8V power supply. The designed VCO is generating a frequency of 3.4 GHz over a temperature range from 0^o C to 65^o C. The VCO has been found to work for all Process (Typical, Slow and Fast corners), Voltage and Temperature (PVT) conditions.

Keywords
Delay cell, Ring oscillator, Voltage Controlled Oscillator, Communication systems.

1. INTRODUCTION
Oscillators are the fundamental part in many electronic systems The High-Definition Multimedia Interface (HDMI) is used for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays **[1].** The required specifications as per the HDMI Specification version 1.4 are given in the **table 1**.

Table 1. HDMI 1.4 specifications

Parameter	**value**
Supply voltage	3.3V
Data rate	3.4GB/s
Tx signal swing(single ended)	400mV to 600mV
Single ended high level output voltage V_H	3.1 V to 3.3 V
Single ended low level output voltage V_L	2.6 V to 2.9V
Rise time/Fall time	>75ps

HDMI requires a 3.4 GHz clock generator circuit to generate data rate at 3.4 GB/s , so the oscillator center frequency should be 3.4GHz.The proposed VCO is achieved 3.4 GHz frequency with wide-tuning rang, better phase noise and work PVT variations. The VCO is designed so that the schematic, layout results are match and should be able to withstand the PVT conditions.

This paper is organized as follows. Section 2 describes the proposed ring VCO. Simulation results are given in Section 3 and the conclusion is given in Section 4.

2. PROPOSED RING VCO
The differential delay stage strength is that ideally noise on the supply appears as common-mode on both outputs and is rejected by next stage in a chain. The VCO is designed using delay cells; the schematic of delay cell is shown in **Fig. 1 and 3**. The delay cell consists of 6 transistors; in this M1 & M2 NMOS input transistors designed for required gain and bandwidth. M5 & M6 NMOS cross coupled transistors to provide positive feedback. M3 & M4 PMOS transistors serving as current source loads and provide designed current for operating frequency. The current is used by the delay cell to produce output frequencies **[2].** The operating frequency is nominally controlled by adjusting the PMOS transistors current. Cross-coupled pairs are adopted to guarantee oscillation with differential outputs. The design is similar to the Lee–Kim delay cell. Unlike the Lee–Kim cell, NMOS transistors are used in the cross-coupled pairs instead of PMOS transistors for a higher operating frequency **[3].** The existence of the zero supply sensitivity and the magnitude of both the positive and negative supply sensitivity depend on the design parameters such as the transistors' width, length and the P/N size ratio of the delay-cell transistors **[4].** The operation of the delay cell can be described as follows: by changing the control voltage on the gate of MP3 and MP4 PMOS transistors the charge up current of the delay cell output load is changed. By changing the channel conductance of PMOS devices, the output frequency can be tuned between maximum and minimum frequency values. By changing the delay time of the delay cells the frequency of the whole VCO is controlled the NMOS cross coupled pair also reduces the supply sensitivity. The dimensions used in delay cell circuit are shown in **table 2.**

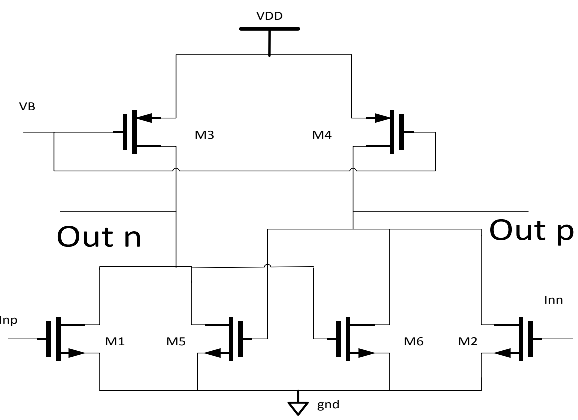

Fig. 1 Schematic of Differential Delay Cell

The complete schematic of the three stage voltage controlled oscillator is illustrated in **Fig. 2**.In this figure M1, M2 and R form a Voltage to Current (V-I) converter, to convert V_{ctrl} to the current. This current acts as a bias current for all 3 delay elements in the VCO circuit.

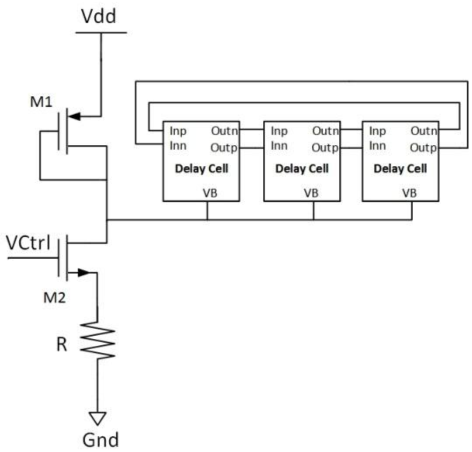

Fig. 2. Schematic of the proposed differential Ring VCO

The control voltage is varied from 0.4 V to 1.6 V. The proposed architecture supports wide-tuning-range also reduces the supply sensitivity.

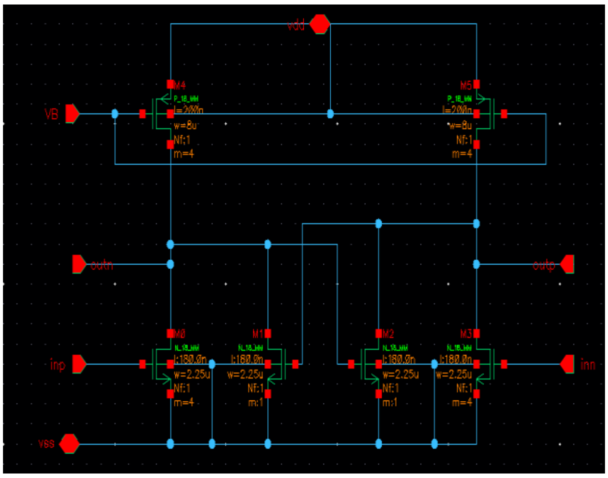

Fig. 3. Differential delay cell

Table 2. Delay cell dimension and descriptions.

Device Name	Dimensions (W/L)	Description
M1 (NMOS)	2.25µm/0.18µm	Input transistors designed for required gain and bandwidth.
M2 (NMOS)	2.25µm/0.18µm	Input transistors designed for required gain and bandwidth.
M5 (NMOS)	2.25µm/0.18µm	Cross coupled transistor to provide positive feedback.
M6 (NMOS)	2.25µm/0.18µm	Cross coupled transistor to provide positive feedback.
M3 (PMOS)	8µm/0.2µm	Load transistor provides designed current for operating frequency.
M4 (PMOS)	8µm/0.2µm	Load transistor provides designed current for operating frequency.

The complete schematic of the three stage voltage controlled oscillator is illustrated in **Fig. 4**.In the test set up V-I converter is used to convert V_{ctrl} to the current the current in each delay cell is 2.5mA.The dimensions used in current source circuit is shown in **table 3.**

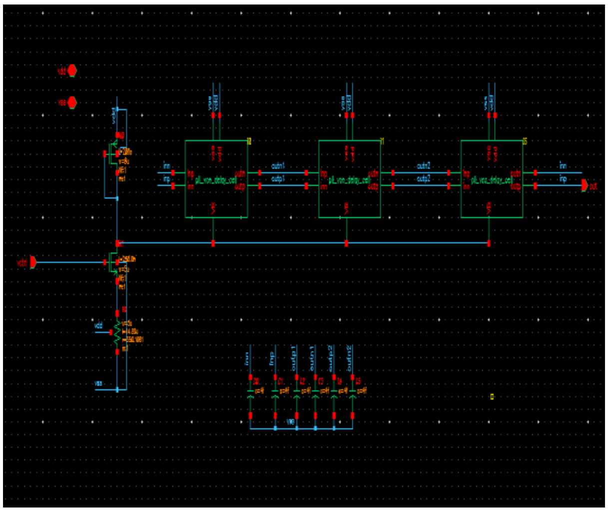

Fig. 4. Three stage Ring VCO Test set up

Table 3. Transistors, resistor dimensions and descriptions in V-I converter in test set-up.

Device Name	Dimensions (W/L)	Description
M1 (NMOS)	8µ/0.2µ	Load transistor provides designed current for operating frequency based upon VCTRL and resistor.
M0 (PMOS)	5µ/0.25µ	Input transistors designed for required gain and bandwidth.
R0 (149.736Ω)	3µ/5µ	Resistor value is shown to operate VCO at 3.4GHz worst case.

3. SIMULATION RESULTS

The process corner simulations were performed on the VCO to determine its performance under different operating conditions**.** The typical corner (TT) was simulated with supply of 1.8V at 27 °C. The fast corner (FF) was simulated with supply of 1.9V at 0 °C and the slow corner (SS) was simulated with supply of 1.7V at 65 °C. The VCO has been found to work under Process, Voltage and Temperature (PVT) conditions. The variation of VCO frequency at process corners is shown in **Fig. 5.** The results illustrates that the operating frequency of the VCO is from 2.2 GHz to 4 GHz. The test case setup is done by sweeping the control voltage from 0.7V to 1.2V and performed the transient analysis to capture the linearity of the voltage controlled oscillator. The gain of the VCO is 3.4 GHz/V i.e., (1.7 GHz/0.5V).

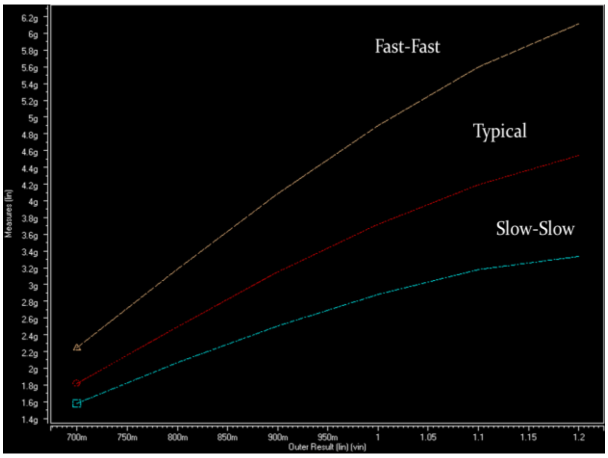

Fig. 5. Variation of VCO frequency at process corners

In **Fig. 6** the results illustrate that for operating frequency of VCO 2.2 GHz to 4 GHz the corresponding current.

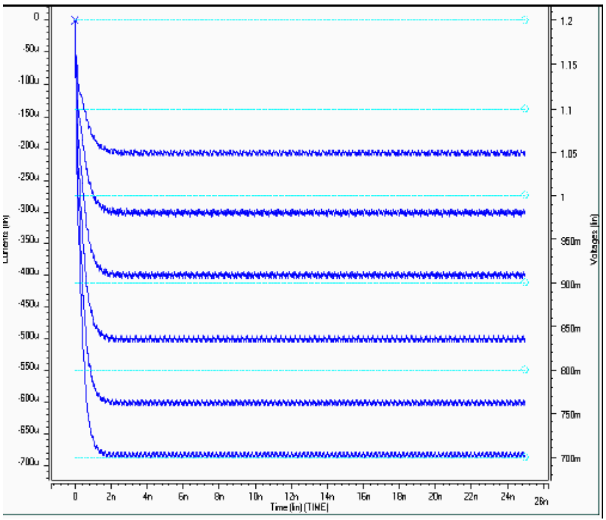

Fig. 6. VCO control voltage Versus Current

In **Fig.7** results illustrate VCO output frequency of 4 GHz. The test case is done by giving 1.1V control voltage and transient analysis is performed.

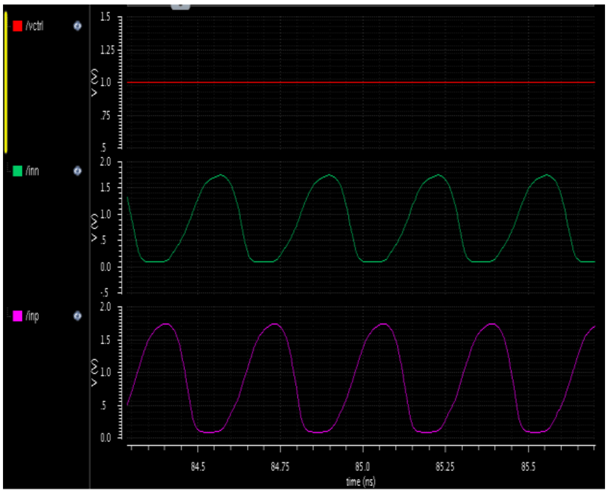

Fig. 7. VCO differential output frequency of 4GHz

In **Fig.8** the results illustrate power supply current at VCO output frequency of 4 GHz. The test case is done by giving 1.1V control voltage and transient analysis is performed.

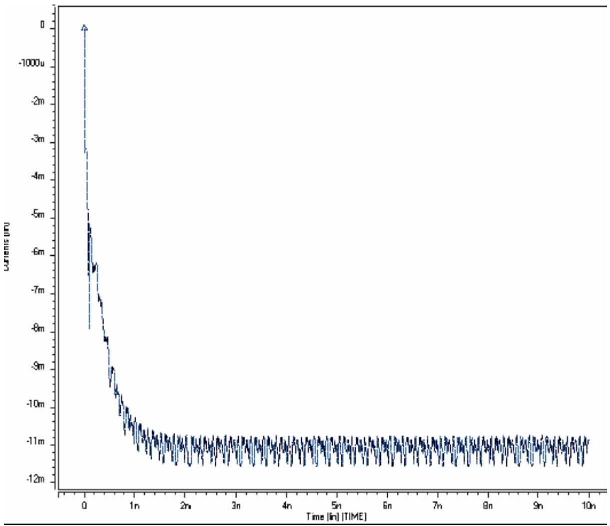

Fig. 8. Power supply current at VCO operating of 4GHz

Table 4 shows that control voltage versus frequency of VCO. The linearity is achieved over a range of frequency from 1.76 GHz to 3.4 GHz. The transistor goes from saturation to triode region if the control voltage crosses 1.15V. So the output frequency of the VCO varies in a nonlinear fashion. In the 3.4 GHz range the VCO is linear.

Table 4. Control voltage versus frequency of VCO

Control Voltage (V_{ctrl})	**Frequency (GHz)**	**Difference (GHz)**
0.4	0.043	-
0.5	0.22	-
0.6	0.6	-
0.7	1.13	0.53
0.8	1.76	0.63
0.9	2.417	0.657
1	3.048	0.631
1.1	3.616	0.568
1.2	4.098	0.482
1.3	4.4769	0.3789
1.4	4.733	0.2561
1.5	4.9	0.167
1.6	4.99	0.09

The phase noise of the Proposed VCO is -140 dBc/Hz (SS-corner) at 3.5 GHz is shown in **Fig. 9.**

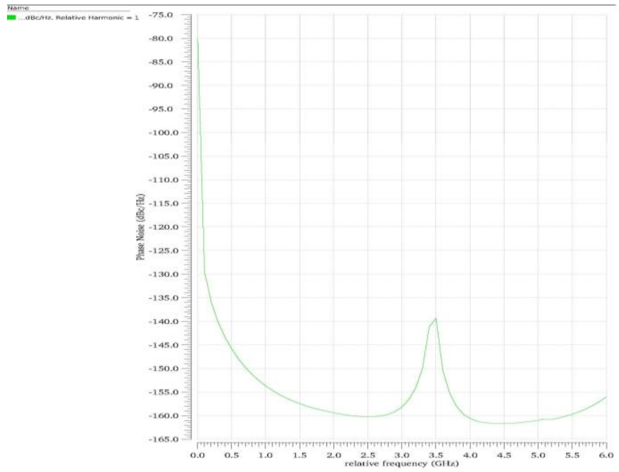

Fig.9. Simulated Phase noise at 3.5GHzfor different relative frequencies

Table 5 shows that performance summary of the proposed VCO. The designed VCO is generating a frequency of 3.4 GHz over a temperature range from 0^o C to 65 ^{o} C, the linearity is achieved over a range of frequency from 1.5 GHz to 3.8 GHz with 60.52% tuning rang. The gain of the proposed VCO is 3.4 GHz/V.

Table 5. Performance summary of the proposed VCO with process corners.

VCO parameters/Process corners	**TT**	**SS**	**FF**	**FNSP**	**SNFP**
Control voltage (Vctrl) (V)	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**
Frequency (GHz)	3.42	2.8	4	3.52	3.28
Linearity (GHz)	1.76 to 3.4	1.5 to 3.8	2.5 to 5.2	2.2 to 4.58	1.9 to 4.8
Tuning range (%)	48	60.52	51.9	51.9	60.4
output Noise (dBc/Hz) @3.4GHz	-133	-135	-132	-118	-108
Phase Noise (dBc/Hz) @3.4GHz	-138	-140	-136	-124	-116
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8

The layout of the proposed delay cell and VCO is shown in **Fig. 10 and 11** respectively**.**

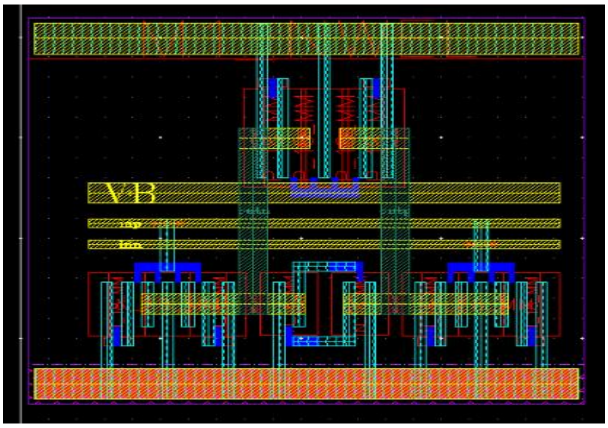

Fig. 10.Layout of proposed delay cell

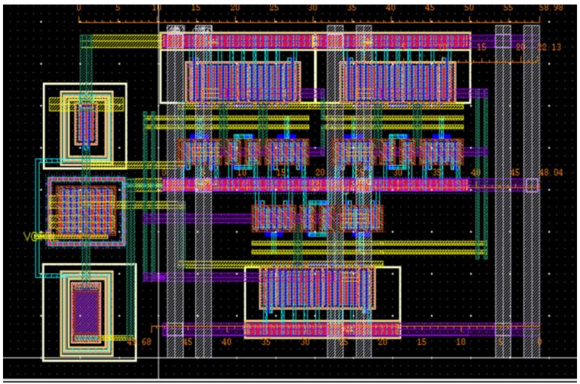

Fig. 11. Layout of proposed VCO

Fig.12 shows the RC (Resistor-Capacitor) extraction of the proposed vco. The number of components present in the extracted view is given in the **table 6.**

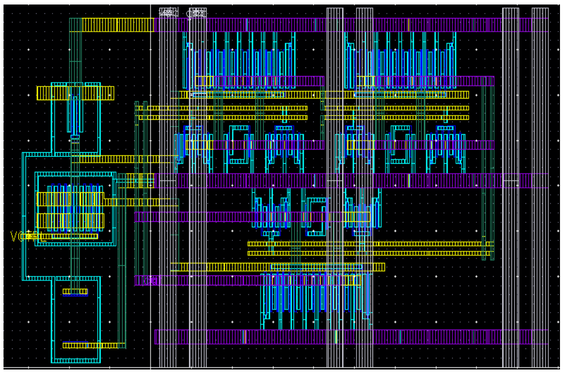

Fig. 12. Extracted view of proposed VCO

Table 6 . Number of components in the extracted view of VCO

Component name	**Number of components**
NMOS Transistors	50
PMOS transistors	56
Resistor	1
Capacitor	6
Paracitic Capacitors	3112
Paracitic resistors	730

Table 7 shows that performance summary and comparison with recently published VCOs. The designed VCO is generating a frequency of 3.4 GHz and the linearity is achieved over a range of frequency from 1.5 GHz to 3.8 GHz with 60.52% tuning range.

Table 7 . Performance summary and comparison with recently published VCO

4. CONCLUSION

In this paper a three stage ring VCO is designed using differential delay cell in 0.18-µm CMOS process under the supply voltage of 1.8 V. Carefully choosing the components W/L values, the VCO oscillate around center frequency of 3.4GHz. All resistances and capacitances were extracted from layout such that we can simulate the circuits more accurately with post layout simulations. All transistors in the present design have been sized appropriately to achieve the targeted design. The VCO has been found to work under Process, Voltage and Temperature (PVT) conditions.

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