Transistor Realization of Reversible Carry Skip Adder Circuits

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ABSTRACT
In today's world , power dissipation is one of the major concern as the complexity of the chip is increasing and more devices are being integrated on a single chip. Thus this high density of chip and increased power dissipation demands for better power optimization methods. Reversible logic is one of the method to reduce power dissipation. Reversible computing has a wide number of applications in areas of advance computing such as low power CMOS VLSI design, nanotechnology, cryptography, optical computing, DNA computing and quantum computing. This paper presents improved and logic efficient reversible four bit carry skip adder block. The performance of the proposed architecture is better in terms of number of transistors, garbage outputs, constant inputs and gate count when compared with existing works. Also the design forms the basis for different quantum ALU and reversible processors.

Keywords
Low Power VLSI, Reversible logic, Carry Skip Adder, quantum ALU.

1. INTRODUCTION
The operation carried out in conventional computers is irreversible i.e the input bits are lost once the output bits are generated by the logic block. Thus irreversible hardware computation causes energy dissipation due to bit loss which is the major issue in future, if technology scaling continue following Moore's law. According to Landauer [1],the loss of each bit of information dissipates minimum kTln2 joules of energy(heat) where $K=1.38060\times10^{23}$ $m^2kg^{-2}K^{-1}$ (joules $Kelvin^1$) is the Boltzmann's constant and T is the absolute temperature at which operation is performed. The erasure done is not significant and hence a lot of power dissipation takes place. And this dissipation is one of the major problem in modern CMOS technology. Thus reversible logic came into existence, which does not lose information and hence dissipate very less heat as compared to classical irreversible logic gates. C.H. Bennett [2] proposed a theoretical background about the reversible logic which give rise to the concept of reversible logic.

Logical reversibility is the possibility to retrace each step and recover the data which was used in every step after a computation is finished. Thus reversible logic circuits offers better alternative solution that allows computation with minimum energy dissipation [3].

According to Frank [4], a small fraction of the energy can be reused by the reversible logic based computers that theoretically can approach approximately near to 100% as the hardware quality is improved.

This paper proposes transistor realization of reversible four bit carry skip adder circuit with the help of basic reversible gates i.e Peres gate, Toffoli gate and Fredkin gate. The rest of the paper is organized as follows: Section 2 provides basic reversible gates present in the literature and their qualitative parameters. Section 3 describes the transistor realization of Peres gate and its full adder implementation. Section 4 illustrates about proposed four bit carry skip adder block and it's comparisons with the existing research works. Finally section 5 concludes the paper.

2. BASIC REVERSIBLE GATES
A reversible function has unique mapping between its input and output, that is, for every output pattern there is an unique input pattern. Also the reversible logic gates are constructed with equal number of inputs and outputs. Reversible logic does not allow fanout and feedback in construction of reversible circuits. This section concentrates on qualitative parameters of reversible gates and also forward and backward computation of basic reversible gates.

2.1 Qualitative Parameters (Cost metrics)
In order to measure the performance of reversible circuits, there are a number of quantitative parameters that are defined below.

2.1.1 Quantum cost(QC):
This gives the number of primitive gates (1×1 or 2×2) used in the quantum logic synthesis of reversible gates. The quantum cost of 1×1 i.e NOT gate and 2×2 gate is taken as unity [5].

2.1.2 Garbage Outputs(GO):
This refers to those outputs which are not primary outputs. These are the additional outputs that are not used in any further computations. In other words these are required to restore reversibility in the circuit and since they remain unused, to make it realizable it is required that this number remains low in a circuit.

2.1.3 Constant Inputs(CI):
Also known as ancilla inputs (0 or 1) i.e ancilla bits. They exists in reversible design to synthesize the given logical function. Like garbage outputs, the number of constant inputs should be minimum.

2.1.4 Delay:
This is basically the total time required to perform a function. From any input line to any output line, the maximum number of gates in this path is considered as delay of the path [6].

2.2 Forward and Backward Computation of Reversible Gates
There are several reversible gates that have been designed. Some basic reversible gates and their quantum equivalent is shown as under.

Fig. 1 shows a Feynman gate [7].As fanouts are not allowed in reversible logic, the required outputs duplication is done by Feynman gate. Hence Feynman gate is also called as Copying gate. The gate has a quantum cost of 1.

Forward Computation:

P=A;

If A=0 then Q=B,

Else Q=B'

Backward Computation:

A=P;

If P=0 then B=Q,

Else B=Q'

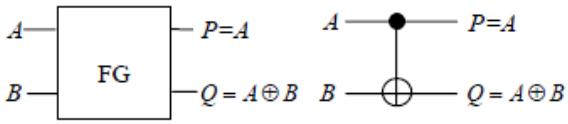


Fig 1: 2×2 Feynman Gate

Fig. 2 shows a 3×3 Toffoli gate [8].It has the quantum cost of 5. Forward Computation:

P=A; Q=B

If A AND B =0 then R=C,

Else R=C'

Backward Computation:

A=P; B=Q;

If P AND Q=0 then C=R,

Else C=R'

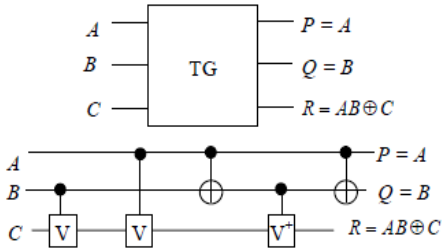


Fig 2: 3×3 Toffoli Gate

Fig. 3 shows a Fredkin gate [9]. It has also the quantum cost of 5.

Forward Computation:

P=A;

If A=0 then Q=B and R=C,

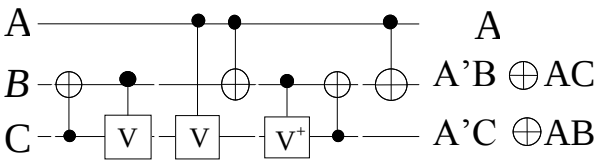
Else Q=C and R=B.

Backward Computation:

A=P;

If P=0 then B=Q and C=R,

Else C=Q and B=R.



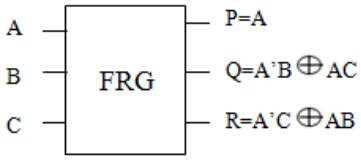


Fig 3: Fredkin Gate

Fig. 4 shows a Peres gate (PG) [10] which is also known as new Toffoli gate. It is the combination of both Feynman and Toffoli gate and has the quantum cost of 4.

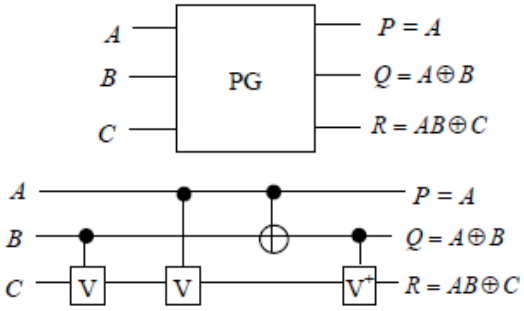


Fig 4: Peres Gate

3. TRANSISTOR REALIZATION OF PERES GATE AND ITS FULL ADDER IMPLEMENTATION

The reversible Peres gate is used to design the proposed carry skip adder block by implementing two peres gate as a full adder block. The transistor implementation of Peres gate is shown in Fig.5 which uses 10 transistors. The block diagram of two peres gates for full adder implementation is shown in Fig.6 and Fig.7.Peres gate is used basically because the full adder implementation of peres gate uses only 17 transistors also it has lowest quantum cost of 4.

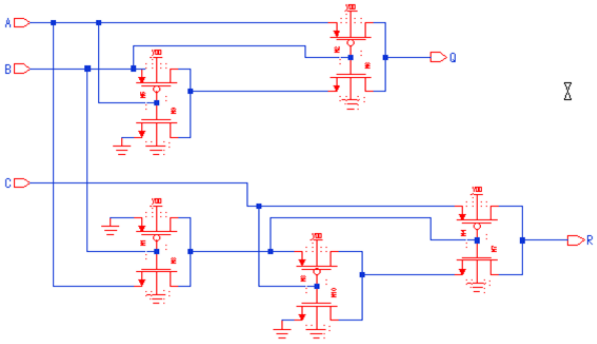


Fig 5: Transistor implementation of Peres gate

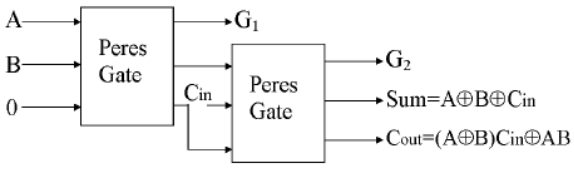


Fig 6: Block diagram of reversible full adder[]

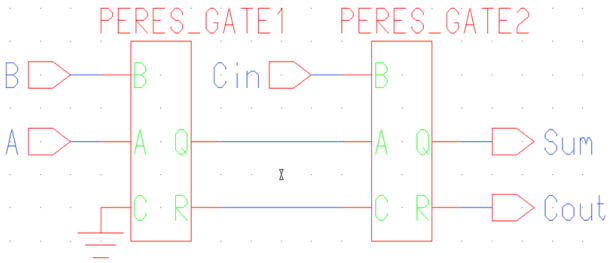
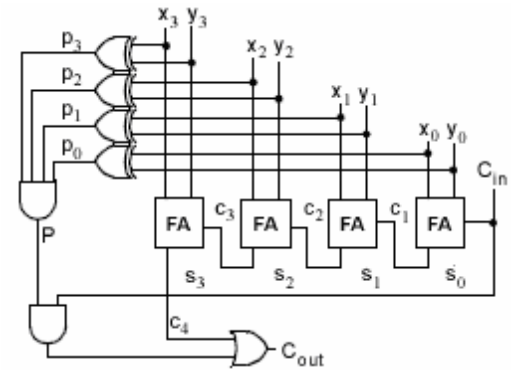


Fig 7: Transistor implementation full adder using two peres gates

4. PROPOSED DESIGN OF FOUR BIT CARRY SKIP ADDER BLOCK

There are several types of adders used in the computing systems and the most common among them is ripple carry adder in which full adders are connected in series and carry is propagated through all the stages and hence requires more carry propagation time to generate carry output [11].Carry look ahead adders are fastest among all the adders since carry output is generated in parallel computation but requires a large number of gates. The carry skip adder shown in Fig 8,is the most promising adder which presents hardware and performance compromise between both the above adders. In the full adder operation, if either of the input is logical one, then the cell will propagate the carry input to carry output. Hence the ith full adder carry input C_i, will propagate to its carry output, C_{i+1}, when $P_i=X_i \oplus Y_i$ [13].

In the proposed carry skip adder in Fig.12, 4 bit parallel addition is done using two peres full adder block as given in Fig.7.The block propagate signal P is generated using three toffoli gates, where $P= p_0.p_1.p_2.p_3$ and $p_0= X_0 \oplus Y_0$, $p_1= X_1 \oplus Y_1$, $p_2= X_2 \oplus Y_2$ and $p_3= X_3 \oplus Y_3$ [14].Here toffoli gates are used because for generating the AND function will reduce the computational complexity of the circuit in terms of transistor implementation without affecting the garbage as the ANDing operation using toffoli gates requires only three transistors when it's third input bit is 0 as shown in the Fig 10.The ORing operation is done by Fredkin gate,its transistor implementation is shown in Fig 11.



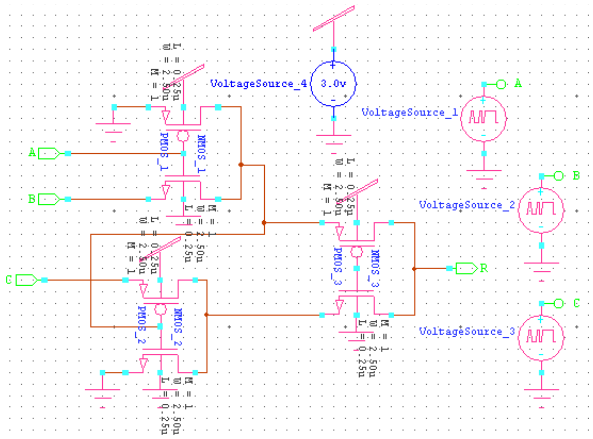


Fig 8: Four bit carry skip adder block[13]

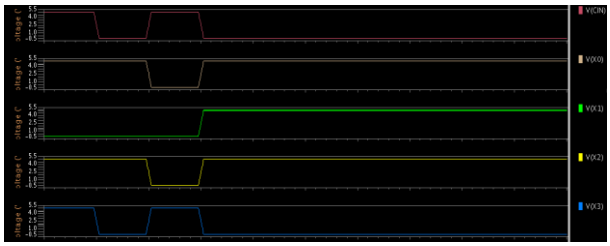
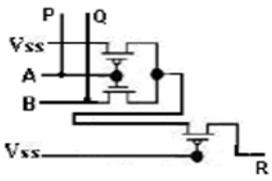


Fig 9: Transistor implementation of Toffoli gate



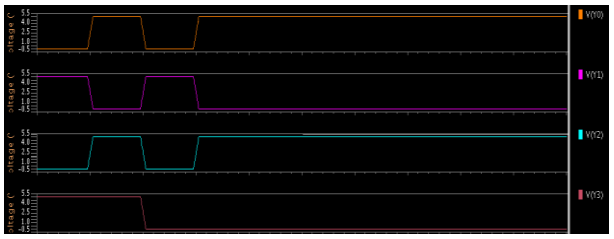


Fig 10: Toffoli gate as a reversible AND gate[13]

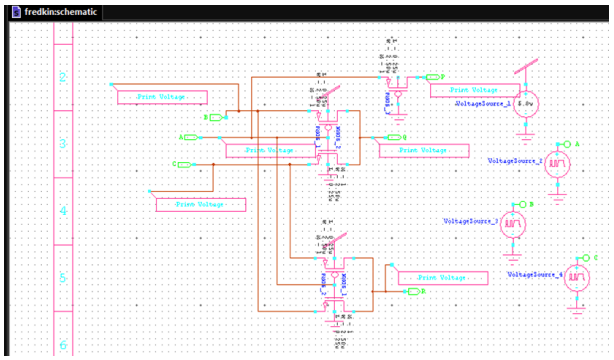


Fig 11: Transistor implementation of Fredkin gate

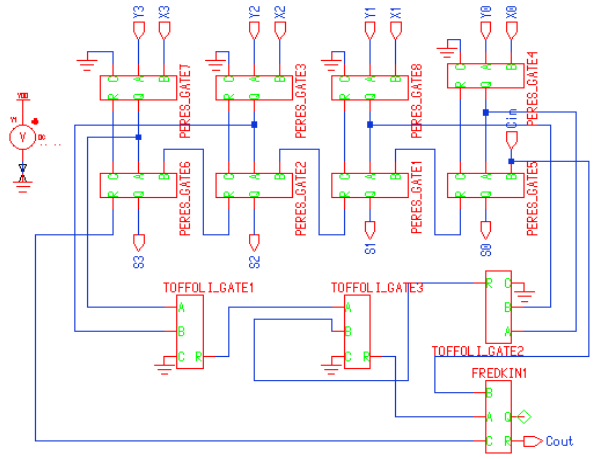


Fig 12: Four bit carry skip adder using Peres gates,Toffoli gates and Fredkin gate

Proposed carry skip adder block constructed with 8 peres gates, 3 Toffoli gates and 1 Fredkin gate. Here the Peres full adder block consists of 2 Peres gates and thus 8 Peres gates are required to generate different propagate signal and three Toffoli gates are used for generating the AND operation,which was required to generate block propagate P signal. Fredkin gate is used to generate an AND and OR operation to generate Cout [14].Simulation result of four bit Carry Skip Adder block is shown in Fig.13. The first waveform is the input bits X_0, X_1, X_2, X_3 , the second waveform is the input bits Y_0, Y_1, Y_2, Y_3 and the third waveform is the output bits S_0, S_1, S_2, S_3 along with the carry output Cout.

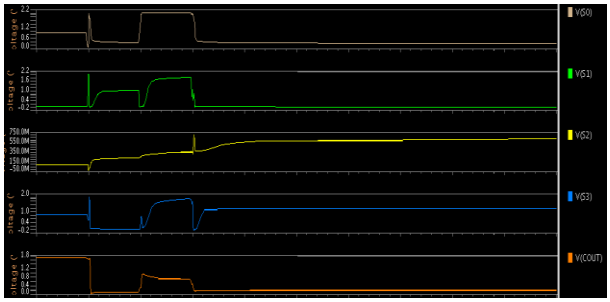


Fig 13: Simulation Results of Four bit Carry Skip Adder block using Peres, Toffoli and Fredkin gates

Table 1. Comparitive Result of Different Four bit Carry Skip Adder Circuit

Adder Designs	Number of gates used	Number of garbage outputs	Number of transistors	Number of constant inputs
Proposed Circuit	**12**	**12**	**81**	**7**
Existing Circuit [11]	**22**	**27**	**264**	**22**
Existing Circuit [12]	**8**	**12**	**85**	**7**
Existing Circuit [13]	**8**	**12**	**85**	**7**
Existing Circuit [14]	**8**	**15**	**91**	**10**
Existing Circuit [15]	**8**	**12**	**88**	**7**

5. CONCLUSION

The key contribution of this paper were carried out for the transistor realization of Four bit Carry Skip Adder Block using Peres gates,Toffoli gates and Fredkin gate with minimum number of transistors. Methodology used for designing reversible gate is Pyxis, Mentor Graphics Tool and technology used is 130nm.It is proved that the proposed design is better than existing circuits in terms of number of transistors used, garbage outputs and constant inputs used. The proposed design find its use in building reversible processor, reversible ALU, etc. Also in quantum computers, this work plays a significant step towards making more complex reversible sequential circuits so as to minimize the power consumption and build more improved applications. However more synthesizing methods are needed to minimize number of constant inputs and garbage outputs. Although there is shortage of simulation, synthesis, testing and verification tools for designing reversible circuits, a lot of research work have been done and still in progress in this direction.

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