Implementation of Leading One Detector based on Reversible Logic for Logarithmic Arithmetic

Durgesh Nandan
Research scholar
Department of Electronics and Communication Engineering
Jaypee University of Engineering and Technology
Guna, Madhya Pradesh, India

Jitendra Kanungo
Assistant Professor
Department of Electronics and Communication Engineering
Jaypee University of Engineering and Technology
Guna, Madhya Pradesh, India

Anurag Mahajan
Assistant Professor
Department of Electronics and Communication Engineering
Jaypee University of Engineering and Technology
Guna, Madhya Pradesh, India

ABSTRACT
Nowadays computers are more efficient and more complex than their predecessors. But, there is some penalty of each and every advantage in the field of technology. Here, penalty comes in terms of power consumption. According to Moore's law, primary reasons for the rise in power consumption are the increase in clock frequency and the increased number of transistors packed onto in same die area. Reversible logic provides high speed and less power consumption. So, it has been widely used in designing of digital circuits for low-power and high-speed computation. Design of Leading One Detector (LOD) is an important circuit as they are used for the normalization process in floating point multiplication, logarithmic multiplication, and in logarithmic converters as useful components. In this paper, we designed a novel LOD based on reversible logic. In order to construct leading-one detector, the innovative reversible Feynman gate (FG) and a special case of TKS gate are proposed. The 4-bit, 8-bit, 16-bit and 32-bit LOD are designed based on the above blocks and some existing reversible gates. VHDL programmed for LOD have been modeled. According to the simulation results, our circuit's logic structures are validated. In terms of Ancillary inputs, garbage outputs quantum cost and delay are compared with the reported works. It can be concluded that our designs perform better than the others. There is no doubt that these can be used as an important component the upcoming low-power quantum computing systems.

General Terms
Reversible logic, Quantum computing, Logarithmic arithmetic Leading one detector.

Keywords
Leading one detector, Reversible logic, Feynman gate, TSK gate, Quantum computing.

1. INTRODUCTION
Advance computers are available in the market with the advancement in the technologies, resulting in faster switching speed. Usually, every technology has limitations and penalties. Here, penalty comes in terms of power consumption. According to Moore's law, primary reasons for the rise in power consumption are the increase in clock frequency and the increased number of transistors packed into a die area. In 1960, Landauer proves that any irreversible circuits can change his state from zero to one and vice-versa. It is directly proportional to the loss of energy [1]. He proposed an equation is for

Loss of energy for each bit of information I_e =KT × ln2 Joule

Where K = Boltzmann constant

T = Temperature at which the system is operating

In 1973, Bennett proved that power dissipation is near to zero if the system were able to return to its initial state from its final state regardless of what happened in the process [2]. Irreversible hardware computation results in energy dissipation due to the loss of information. The logic gates do not loose information is called reversible logic gate and lossless circuit [3].

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backward or un-computing the results. This is termed as logical reversibility [4]. The benefits of logical reversibility can be gained only by employing physical reversibility. Physical reversibility is a process that dissipates no energy in the form of heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency [4].

Reversible logic has the ability to provide high speed outputs and less power consumption. So, nowadays it is an emerging field to design the low-power and high-speed arithmetic computation. Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation for low power VLSI design. Reversible computing may have applications in computer security, Quantum computer, Nanotechnology, Optical computing, bioinformatics, communication, quantum-dot cellular automata computer graphics, cryptography, information security ,design of low power arithmetic and data path for digital signal processing (DSP), Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power [5-10]. Quantum cost, delay, garbage output and a number of gates used in a reversible design should be kept as minimum as possible [11].

Design of LOD is important as they are used for the

normalization process in floating point multiplication, logarithmic multiplication and in logarithmic converters [12-17]. In this paper, we have designed the novel reversible LOD. In order to construct LOD, a special case of Feynman gate (FG) and a special case of TKS gate are proposed. The 4-bit, 8-bit and16-bit LOD are designed based on the above blocks and some existing reversible gates. According to the simulation results, our circuits' logic structures are validated. The important cost metrics of Ancillary inputs (AI), Garbage outputs (GO), Quantum cost (QC) and delay are compared. It can be concluded that our designs perform better than the others. There is no doubt that they can be used as an important component to apply in upcoming low-power quantum computing systems. The rest of paper is arranged as follows: Section II gives the idea about the basic reversible gate and review for systematic growth of existing approaches. Section III, we have briefly discussed the available designs of LOD. Our proposed method and reversible logic architecture are described in Section IV. Section V explores the results. Finally, the finding of the LOD using reversible logic exploration is concluded in Section VI.

2. LITERATURE REVIEW OF REVERSIBLE GATES

In this section, we present the basic idea of well known and frequently used reversible gates which are capable of implementing digital circuits and the systematic development of several reversible gates.

2.1 Reversible Gates

Many reversible logic gates are available in the market. In this section, we discuss those gates which are basic reversible gates. It can be classified into four categories based on the number of inputs and number of outputs in a gate.

(1) 1 × 1 gate: The gate which has only 1 input and 1 output fall in this category. 1 × 1 NOT gate is the only gate which lies in this category. It represented as shown Fig.1. It has 1 quantum cost [17].

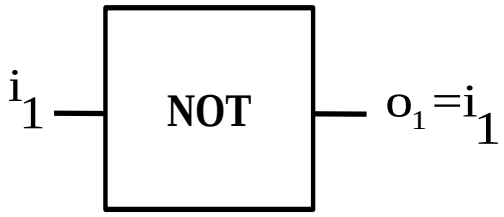
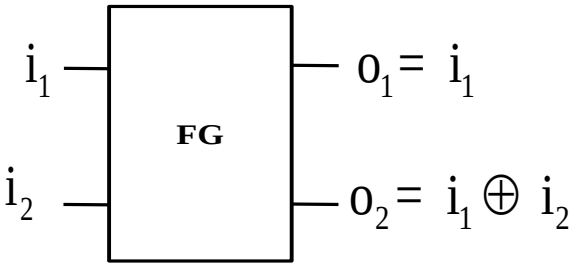
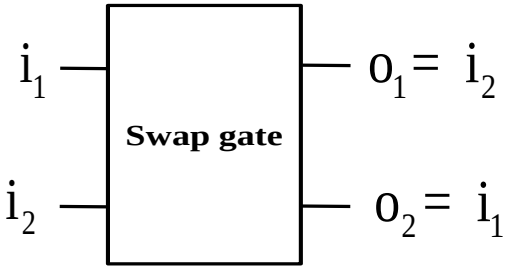


Fig. 1: NOT gate

(2) 2 × 2 gates: The gate which has 2 inputs and 2 outputs fall in this category. Like 2 × 2 Feynman gate (CNOT gate) and 2 × 2 swap gate (SG) [18-20]. Feynman gate is also called controlled NOT gate or CNOT gate because input 1 controls the behavior of output 1 and 2. It has 1 QC. SG is used for interchanging the position of input at output position. QC of SG is 3. It represented as shown Fig.2 (a) for Feynman gate and 2(b) for swap gate.



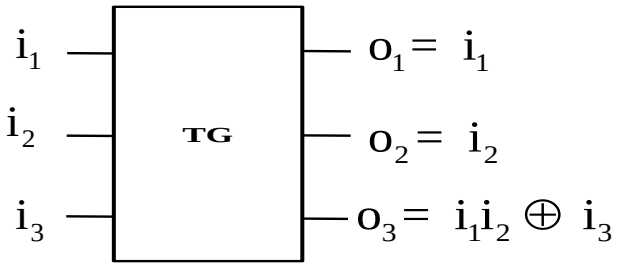
(a)



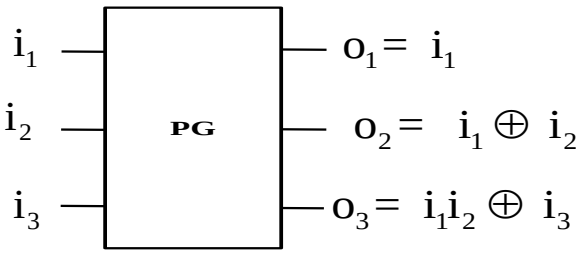
(b)

Fig. 2: (a) Feynman gate and (b) Swap gate

(3) 3 × 3 gates: The gate which has 3 inputs and 3 outputs fall in this category. Mostly gate falls in this category, Like 3 × 3 Feynman Double Gate (F2G), 3 × 3 Toffoli Gate (TG), 3 × 3 Modified Toffoli Gate (MTG), 3 × 3 Peres Gate (PG), 3 × 3 Fredkin Gate (FRG), 3 × 3 Modified Fredkin Gate (MFRG), 3 × 3 TKS Gate, 3 × 3 New Gate and many more [17-20]. TG is the universal gate, it can be used to produce other digital logic gates like AND, OR, NAND etc. QC of TG is 5 and QC of PG are 4.New gate is also used as a universal gate. FRG is used as a controlled swap gate. QC of FRG is 5. TKS can be used to implement a 2×1 multiplexer. It is two output function as a 2×1 multiplexer. It is represented in Fig.3 (a) for Toffoli Gate, 3(b) for Peres Gate, 3(c) for Fredkin Gate, 3 (d) for New Gate and 3(e) for TKS Gate.



(a)



(b)

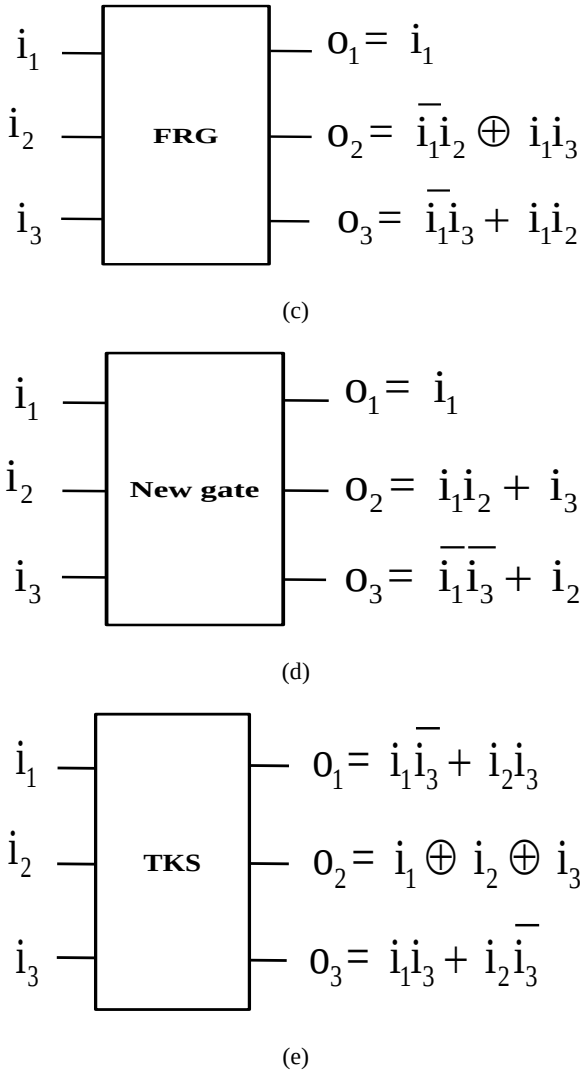


Fig. 3: (a) Toffoli Gate, (b) Peres Gate, (c) Fredkin Gate, (d) New Gate and (e) TKS Gate

(4) 4 × 4 gates: The gate which has 4 inputs and 4 outputs fall in this category. 4 × 4 HNG, 4 × 4 BVF Gate, 4 × 4 TS Gate, 4 × 4 Sayen Gate, 4 × 4 DKG Gate, 4 × 4 NC Gate are few example of 4 × 4 gate and many more example are available in the literature [17-20]. Mostly, these gates are developed to form the special digital circuits as for full adder, half adder, full subtractor, nine complements etc.

The main motive of this paper is to implement the reversible logic for LOD, So at first, we try to understand about the LOD, its work and its architecture. LOD is briefly described in next section.

3. LEADING ONE DETECTOR

Design of leading-one detector is important components where high performance and speed are the main concerns in digital circuit design. It is used for the normalization process in floating point multiplication, logarithmic multiplication, and in logarithmic converters as useful components. LOD is used in logarithmic converters to find the integer portion and the fractional part of the binary logarithm. The 4-bit and 16-bit LOD circuits are shown in Fig. 4 and Fig.5 respectively. It evaluates the LOD from the MSB (d3) to the LSB (d0) a 4-bit LOD. Then with 4-bit LOD, we can design the 16-bit LOD.

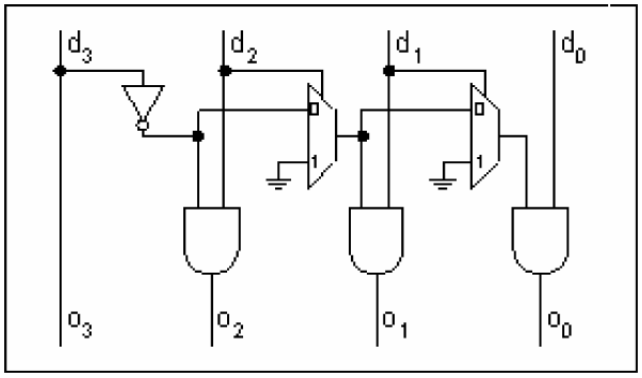


Fig. 4: 4 bit LOD circuit [21]

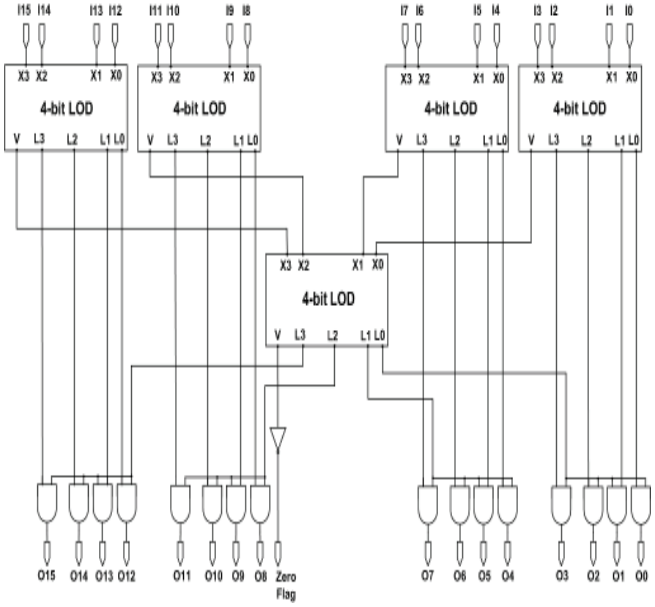


Fig 5: 16 bit LOD circuit [22]

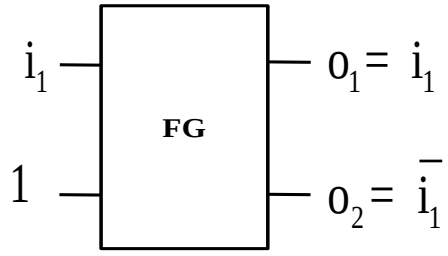
4. PROPOSED DESIGN OF REVERSIBLE N-BIT LEADING ONE DETECTOR

We propose reversible n-bit LOD to the best of our knowledge it is first time proposed. A LOD determines the leading one position. To construct the n-bit LOD, we have used two special case reversible gates, name as a special case of FG and TKS gate in Sections 4.1. Section 4.2 shows the design of reversible 4-bit LOD circuit and design of reversible n-bits LOD circuit.

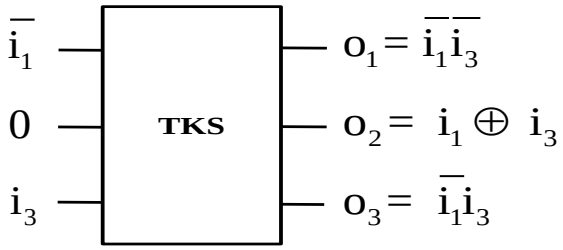
4.1 Proposed special condition of FG and TKS gate

In this subsection, we show the special condition of 3 × 3 reversible Feynman gate and 3 × 3 reversible TKS gate. It is shown in Fig. 6 (a) and (b). The truth table of the special condition of 3 × 3 reversible Feynman gate is given in Table 1. It can easily be verified that the input pattern and output pattern uniquely performed the reversibility. The proposed special condition of 3 × 3 reversible Feynman gate is implemented for all Boolean functions. For example, let inputs are i_1 and i_2, then outputs $o_1 = i_1$ and $o_1 = \bar{i}_1$. FG gate is used to design the MSB of 4-bit LOD. The truth table

of the special condition of 3 × 3 reversible TKS gate is given in Table 2. It is easily verified that the input pattern and output pattern for a special condition of 3 × 3 reversible, TKS gate uniquely performed the reversibility. The proposed special condition of 3 × 3 reversible Feynman gate is implemented for all Boolean functions. When inputs are $\bar{i}_1$, 0 and i_3, then outputs are $o_1 = \bar{i}_1\bar{i}_3$, $o_2 = i_1 \oplus i_2$ and $o_3 = \bar{i}_1 i_3$. We design the n-bit LOD with the help of FG and TKS gate.



(a)



(b)

Fig. 6:(a) Special condition of FG (b) Special condition of TKS gate

Table 1. Truth table of FG

Input value		Output value	
i_1	i_2	O_1	O_2
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 2. Truth table of TKS Gate

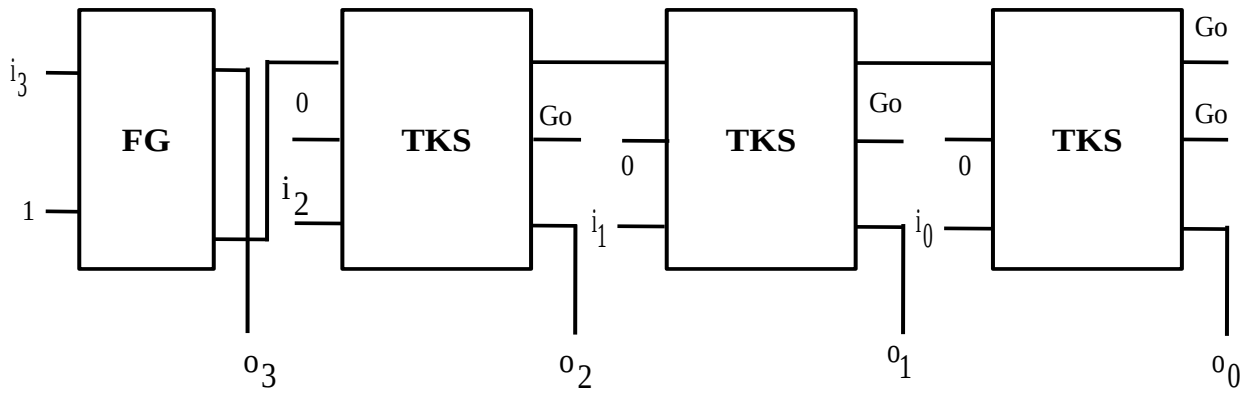
Input value			Output value		
i_1	i_2	i_3	O_1	O_2	O_3
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	1	1	1

4.2 Proposed design of reversible LOD

The proposed design of 4 × 4 reversible 4-bit LOD is shown in Fig. 7(a). It is prepared with the help of FG and TKS gates. FG has 2 inputs, one input to a constant value and producing 2 outputs complement of each other. TKS gate has three inputs and 2nd input value is always zero, giving 2 outputs and one garbage output. The truth table of reversible 4-bit LOD is shown in table 3. From the truth table, it is clear that $o_3 = i_3$, $o_2 = \bar{i}_3 i_2$, $o_1 = \bar{i}_3\bar{i}_2 i_1$ and $o_0 = \bar{i}_3\bar{i}_2\bar{i}_1 i_0$. Generalize design of reversible n-bit LOD is shown in Fig. 7(b).

Table 3. Truth table of 4 × 4 reversible 4-bit LOD

Input value				Output value			
i_3	i_2	i_1	i_0	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0



(a)

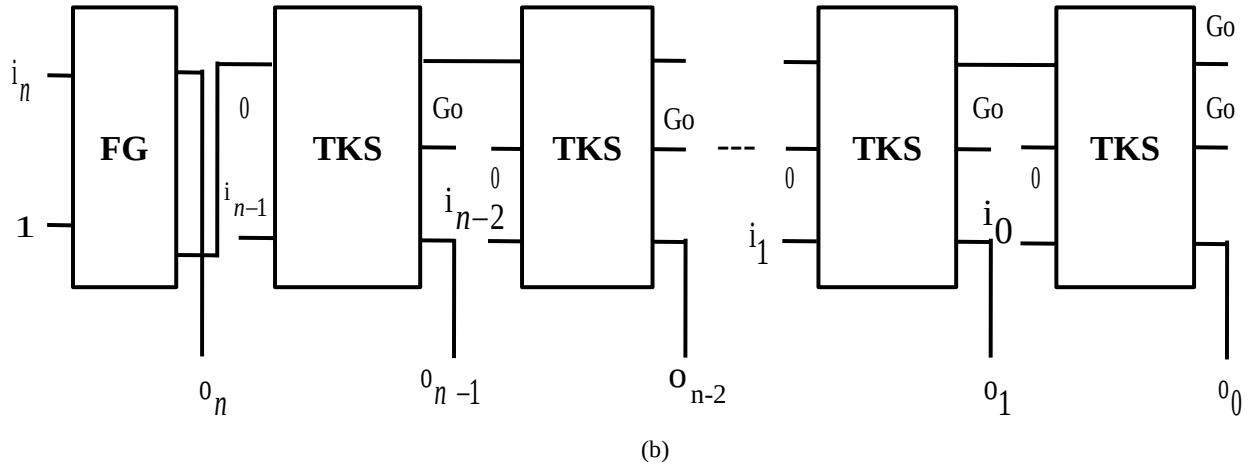


Fig. 7: (a) the design of reversible 4-bit LOD circuit (b) the design of reversible n-bits LOD circuit

5. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

In a synthesis of quantum reversible circuits, it is important to evaluate the designed circuits. For the correctness of logic functions in a circuit, the functional simulations are implemented. The architectures of 4-bit LOD and 16-bit LOD are successfully modeled by using VHDL. VHDL code is carried out on Xilinx ISE Design Suite 12.1. The reversible design of 4-bit LOD and 16-bit LOD are shown in Fig. 8 and 9. In Fig.8, 4-bit LOD is implemented for a 4-bit input. It has constant ancila inputs 1000 and giving 4-bit outputs. In this way, we verified the design for a 4-bit LOD. In the same manner from Fig. 9, 16-bit LOD is implemented for various 16-bit inputs like "1111111111111111", "0111111111111111" etc. it has constant ancila inputs 1000 and we obtain "1000000000000000", "0100000000000000" etc outputs. Thus, the design is verified for 16-bit LOD. The performance of our reversible LOD in terms of QC, Delay, AI and GO are shown in Table 4. The 4-bit LOD gives 16 QC, 16 Delay, 4AI and 3GO found. We obtain 61 QC, 61 Delay, 16AI and 15GO for 16-bit LOD. To implement an architecture generalized the required n-bit LOD 4(n-1) +1 QC, 4(n-1) +1 Delay, n AI and (n-1) GO.

Table 4. Performance of reversible LOD

	QC	Delay	AI	GO
Proposed 4-bit LOD	16	16 Δ	4	3
Proposed 16-bit LOD	61	61 Δ	16	15
Proposed n-bit LOD	4(n-1)+1	4(n-1)+1 Δ	N	n-1

6. CONCLUSIONS AND FUTURE WORK

In this paper, we purpose efficient methods to design quantum reversible n-bit LOD. The 4-bit LOD, 16-bit LOD and n-bit LOD are the first time implement by using reversible logic literature. The proposed designs are analyzed in terms of QC, delay, AI and GO. The correctness of design has been verified by using VHDL test bench.

Reversible logic based LOD as a component for implementation of logarithmic multiplication, and in logarithmic converters may be a useful component in digital signal processing for the future research challenges.

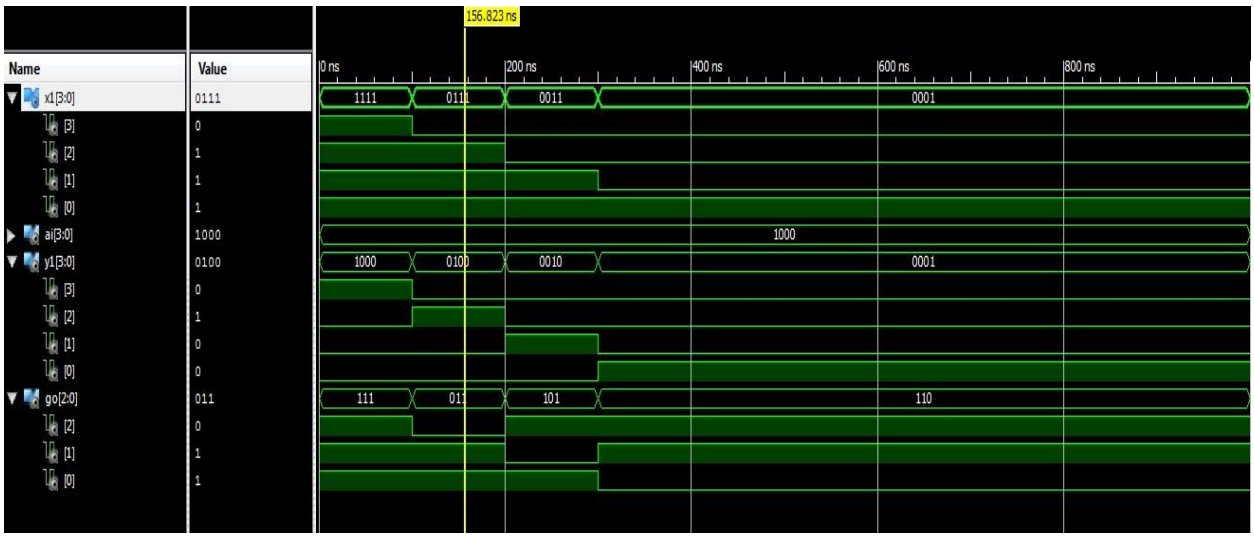


Fig. 8: Functional simulation of reversible 4-bit LOD

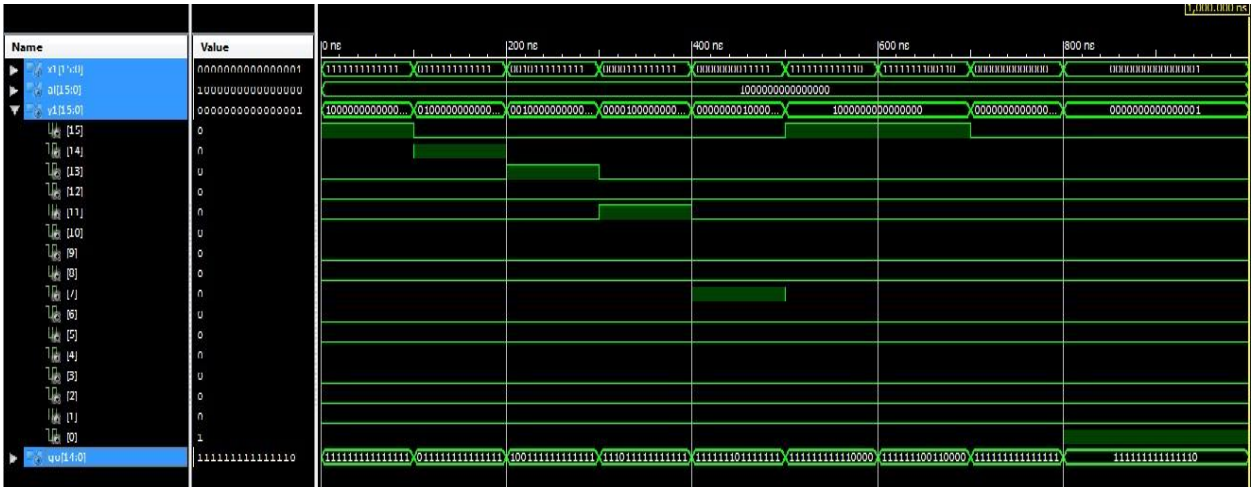


Fig. 9: Functional simulation of reversible 16-bit LOD

7. REFERENCES

[1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp. 183-191, 1961.

[2] C.H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp. 525-532, November 1973.

[3] T. Toffoli, "Reversible computing", Automata, Languages and Programming, 1980, pp. 632-644.

[4] Prashant R. Yelekar and Sujata S. Chiwande, "Design of sequential circuit using reversible logic", IEEE ICAESM, 2012, pp.321-326

[5] M.A. Nielsen and I.L Chuang, "Quantum computation and quantum information", Cambridge University Press, New York, 2000.

[6] V. Vedral, A. Barenco and A. Ekert, "Quantum networks for elementary arithmetic operations", Physical Review, Vol. 54(1), 1996, pp.147.

[7] A.D. Vos, Y.V. Rentergem, "Power consumption in reversible logic addressed by a ramp voltage", In: PATMOS, 2005, pp. 207–216.

[8] I. Ercan and N. Anderson, "Heat dissipation bounds for nanocomputing: theory and application to QCA", 11th IEEE conference on nanotechnology (IEEE-NANO), 2011, pp 1289–1294

[9] N. Anderson, I. Ercan and N. Ganesh, "Toward nanoprocessor thermodynamics", Proceedings of 12th IEEE conference on nanotechnology (IEEE-NANO), 2012, pp 1–6.

[10] K.Stearns, N. Anderson, "Throughput-dissipation tradeoff in partially reversible nano computing: a case study", NANOARCH, 2013, pp. 101–105.

[11] H. Thapliyal and N. Rangantathan "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage outputs," ACM Journal on Emerging Technologies in Computing Systems, 2010, Vol. 6(4), pp. 1-31.

[12] H. Suzuki, H. Morinaka, H. Makino, Y. Nakase, K. Mashiko, and T. Sumi, "Leading-Zero Anticipatory Logic for High Speed Floating Point Addition," IEEE J. Solid-State Circuits, 1996,vol. 31(8), pp. 1,157-1,164.

[13] Durgesh Nandan, J. Kanungo and A. Mahajan, "An efficient VLSI architecture for Iterative Logarithmic Multiplier", IEEE 4th International conference on signal processing and integrated networks (SPIN), 2017.

[14] Durgesh Nandan, J. Kanungo and A. Mahajan, "An efficient antilogarithmic converter by using 11-regions error correction scheme", IEEE 4th International signal processing, Computing and Control (ISPCC), 2017.

[15] Durgesh Nandan, A. Mahajan and J. Kanungo, "An Efficient VLSI architecture design for antilogarithmic converter by using the error correction scheme", IETE International conference on signal processing (ICSP), 2016.

[16] Durgesh Nandan, J. Kanungo, A. Mahajan, "An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition," Elsevier, VLSI the integration journal, 2017, Vol. 58, pp. 134-141.

[17] P. Akhter, S. Bandewar, Durgesh Nandan, "Logarithmic Multiplier: An Analytical Review" International Journal of Engineering Research, 2016, Volume No.5 (8), pp: 721-723.

[18] H. V. Jayashree , Himanshu Thapliyal , Hamid R. Arabnia and V. K. Agrawal, " Ancilla input and garbage-output optimized design of a reversible quantum integer multiplier", Journal of Supercomputer, 2016,Vol.72, pp.1477–1493.

[19] Md. Hafiz, H. Babu, N. Saleheen, L. Jamal, S.M. Sarwar and T. Sasao, "Approach to design a compact reversible low power binary comparator", IET Computers & Digital Techniques, 2014, Vol. 8(3), pp. 129–139.

[20] Himanshu Thapliyal and M.B. Srinivasa, "Novel design and reversible logic synthesis of multiplexer based full adder and multipliers, IEEE, 2005, pp. 1593-1596.

[21] Khalid H. Abed, Raymond E. Siferd, "VLSI Implementations of Low-Power Leading-One Detector Circuits" IEEE Southeast Conference, 2006, pp. 279 – 284.

[22] K. Kunaraj and R. Seshasayanan, "Leading one detectors and leading one position detectors- An evolutionary design methodology", Canadian journal of electrical and computer engineering, Vol. 36(3), pp. 103-110.