Sine and Cosine Generator and FIR Filter Designing based on CORDIC Algorithm

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ABSTRACT
Field Programmable Gate Array (FPGA) technology is the popular platform for the designing of higher speed of algorithms which are used in the field of the signal processing. There are various applications which are designed by the scientist on the FPGA platform such that digital filters, their sampling rates are more than the available digital filter DSP chip. FPGA implemented digital filter has higher flexibility, low cost than the available DSP chips. In Digital signal processing area and VLSI technology there are various algorithm for the production of the high speed VLSI different circuits. Among these the CORDIC algorithm [1, 5] is most popular for the designing of the high speed VLSI architecture. For the reduction of occupied space and energy consumption we design the scale free CORDIC architecture.

This paper proposed a CORDIC pipelined architecture. By this architecture we compute the sine cosine function, and also we design the high pass FIR Filter by using VHDL language. The sine cosine generator and high pass FIR filter have synthesized by using typical and scale free CORDIC algorithm. These designing are simulated and tested on FPGA Virtex 4 device. These codes have synthesized using Xilinx ISim 13.1 simulator software. We also discuss about the total energy consumption, plot of output of the Filter and their analysis. Give the relative examination of the typical CORDIC algorithm and scale free CORDIC algorithm based designing.

General Terms
CORDIC Algorithm, Filter Designing.

Keywords
Scale free CORDIC Algorithm, Finite Impulse Response Filter, and High Pass Filter.

1. INTRODUCTION
The task termed as Filtering is the procedure for extracting of the signals for the particular applications. In VLSI technology the fast digital filters are designed on the FPGA. In the last five to ten decades the CORDIC algorithm is the very eminent algorithm to producing the fast VLSI implementations. It is a productive and capable hardware algorithm to optimizing the area, speed, power and hardware cost. The typical CORDIC (Coordinate Rotation Digital Computer) algorithm is designed by Jack.E.Volder, which is a 3-D rotational vector algorithm. In 1971 unified CORDIC algorithm [2, 6] was invented. It is used in hyperbolic, linear, circular coordinates systems for the computations of several trigonometric functions, hyperbolic function and logarithmic functions of real and complex numbers. For reducing the number of iterations there are abundance of advancements in

CORDIC algorithm, like the angle-recording (AR), modified vector rotation, mixed scaling rotation (MSR) and scaling free CORDIC algorithms. These algorithms have been improving the system performance and speed. In this paper we have discussed about the typical, scale free CORDIC algorithm, CORDIC Architecture [3, 4], FIR filter in section II, III, IV respectively. In section V we have to deal with designing of sine cosine generator & FIR filter based on typical CORDIC algorithm and scale free CORDIC algorithm. In section V we discuss about sine cosine generation by using typical CORDIC algorithm and scale free CORDIC algorithm, total energy consumption, plot of output of the Filter, and comparative analysis of typical and scale free CORDIC algorithm based designing.

2. THEORY OF CORDIC ALGORITHM
The algorithm is defined in such a way that it is an iterative sequence of additions or subtractions and shift operations are used in two different fashion, rotation and vectoring. In the algorithm vector are rotated by a fixed rotation angle in three different coordinate system, circular, linear and hyperbolic system.

2.1 The Typical CORDIC algorithm
is in the general rotation transform-

$$x1 = x\cos\alpha - y\sin\alpha \quad (1)$$
$$y1 = x\sin\alpha + y\cos\alpha \quad (2)$$

The above equations can readjusted as

$$x1 = [x - y\tan\alpha]\cos\alpha \quad (3)$$
$$y1 = [y + xtan\alpha]\cos\alpha \quad (4)$$

These rotation of angles are represented so as $\tan\alpha = \pm 2^{-i}$. The tangent multiplication is reduced by simple shift operation. The angle α divided into elementary rotation angle in a sequence manner.

$$\alpha = \sum \alpha i \quad (5)$$

So iterative equations of CORDIC Algorithm are

$$xi + 1 = [xi - yi\tan\alpha i]\cos\alpha i \quad (6)$$
$$yi + 1 = [yi + xi\tan\alpha i]\cos\alpha i \quad (7)$$

For the trigonometric identities

$$\cos\alpha i = 1/\sqrt{1 + \tan\alpha i^2} \quad (8)$$

Replace the term $1/\sqrt{1 + \tan\alpha i^2} = ki$
or $ki = 1/\sqrt{(1 + 2^{-2i}}$ (9)

ki denotes as constant multiplication factor .The gain is

defined as the inverse of the constant multiplication factor.

$$Ai = 1/ki$$

.

The system gain

$$An = \Pi\left[1 + 2^{-2i}\right] \approx 1.647 \quad (10)$$

So the above equation no. (6) and (7) becomes

$$xi + 1 = ki\left[xi - yi.di.2^{-i}\right] \quad (11)$$
$$yi + 1 = ki\left[yi + xi.di.2^{-i}\right] \quad (12)$$

di is the decision function depends the rotational mode. First is the rotation mode and second is the vectoring mode

a) For the rotation mode

$$di = -1\ if\ zi < 0 \quad (13)$$
$$di = +1\ if\ else$$

After n^{th} iteration it produces the following results

$$xn = An[x0\cos z0 - y0\sin z0\ ] \quad (14)$$
$$yn = An[x0\sin z0 + y0\cos z0\ ] \quad (15)$$
$$zn = 0 \quad (16)$$

b) For vectoring mode

$$di = +1\ if\ yi < 0 \quad (17)$$
$$= -1\ else$$

After n iteration it produces the following results

$$xn = An\sqrt{[(x0^2) + (y0^2]} \quad (18)$$
$$zn = \tan^{-1}(y0/x0) + z0 \quad (19)$$
$$yn = 0 \quad (20)$$

2.2 Scale Free CORDIC Algorithm

The improvements of CORDIC algorithm are very important aspect. There are disparate developments of the CORDIC architectures for high performance and for reduction of the cost. Pipelined and parallel CORDIC architectures are suitable for the high throughput. For high performance and high throughput, radix -2 with constant scale factor using signed digit(SD) arithmetic and carry save arithmetic(cs) are used in CORDIC algorithm, such as double rotation, correcting rotation, branching method, double step branching, differential methods are used.

Radix-4 based CORDIC algorithm is also used for the enhancement of the speed of the CORDIC architectures. By using radix-4 the no of iterations of the CORDIC algorithm are also reduced. It has been developed and reported in the literature by antelo et.al. and lakshmi. Radix -4 based CORDIC architectures [7, 8, and 9] has been occupied larger area and required higher computational time. There are two main directions for the improvements of the CORDIC algorithm (i) higher Radix (b) Scaling factor. It is very important that the CORDIC architectures are designed in such a way that the CORDIC architecture speed is very high but the no of iteration has also been decreased. From last five decades there are some improvements in CORDIC algorithm like scaling free CORDIC algorithm, enhanced scaling free CORDIC algorithm and virtually scaling free CORDIC algorithm. The scaling-free CORDIC algorithm is designed by using the taylor series approximation method, but the area consumption will be increased in this method. The enhanced scale-free CORDIC is the combination of the typical CORDIC algorithm with scaling –free CORDIC algorithm. However this type of mechanism weakens the potential and capability of the system. Virtually modified scaling-free algorithm improves the range of target of the angle over the entire coordinate symmetry.

3. CORDIC ARCHITECTURE

(a)CORDIC ARCHITECTURE: The two main parts of the CORDIC Architecture
(i) Folded
(ii) Unfolded
Folded architecture has two parts Serial and word Serial
Unfolded architecture has two parts Pipelined and parallel.
In this project we use the pipelined architecture.
First of all we use scaled pipelined architecture, and then scale free pipelined CORDIC architecture.

(b)Scaling-free CORDIC [10, 11] is initially designed by using Taylor-series. The sine and cosine approximated to

$$\sin\alpha i = 2^{-i},$$
$$\cos\alpha i = 1 - 2^{-(2i+1)}$$

Taylor series expansion allowed the rotation only in one direction compared to typical CORDIC.

The taylor series of sine and cosine terms defined as

$$\sin\alpha i = \sum_{n=0}^{\infty}(-1)^n \frac{\alpha i^{2n}}{!2n} = 1 - \frac{\alpha i^2}{!2} + \frac{\alpha i^4}{!4} + \text{----------}$$

$$\cos\alpha i = \sum_{n=0}^{\infty}(-1)^n \frac{\alpha i^{2n+1}}{!2n+1} = \alpha i - \frac{\alpha i^3}{!3} + \frac{\alpha i^5}{!5} + \ - - -$$

The suggested algorithm used third order expansion and approximate 3! To 2^3.By this approximation the mean square error in sine cosine values are 0.0168% which is insignificant and does not affect the accuracy of the system performance.

There are two modules for the designing of the scale free CORDIC processor, the Coordinate calculation modules and shift calculation modules.

(i)Coordinate Calculation Modules:-The expansion of the third order Taylor series approximation is as in equations.

$$xi + 1 = \left(1 - \frac{\alpha i^2}{!2}\right)xi - \left(\alpha i - \frac{\alpha i^3}{!3}\right)yi$$
$$yi + 1 = \left(\alpha i - \frac{\alpha i^3}{!3}\right)xi + \left(1 - \frac{\alpha i^2}{!2}\right)yi$$

Assuming $\alpha i = 2^{-si}$ and approximation of factorial, the above equation can be simplified to

$$xi + 1 = \left(1 - \frac{2^{-2si}}{2}\right)xi - \left(2^{-2si} - \frac{2^{-3si}}{2^3}\right)yi$$
$$yi + 1 = \left(2^{-2si} - \frac{2^{-3si}}{2^3}\right)xi + \left(1 - \frac{2^{-2si}}{2}\right)yi$$

$$xi + 1 = \left(1 - 2^{-(2si+1)}\right)xi - \left(2^{-2si} - 2^{-(3si+3)}\right)yi$$
$$yi + 1 = \left(2^{-2si} - 2^{-(3si+3)}\right)xi + \left(1 - 2^{-(2si+1)}\right)yi$$

The above equations are used for calculation for the x and y coordinates. The output of this module will be used as input to the next clock cycle and the iteration continues until the counter is reset to zero.

(ii)Shift Calculation module:-The word length is fixed up to N=16. M is the location of the most significant bit 1 first of the input angle θi. By the help of identification of the location of the first (1) bit of the input string angle (θ) we find out the shift index value for next calculation of the coordinate. α is the first elementary angle=0.25. Total no of iteration for third order taylor series is 7 and shift calculation module is used to get the shift index (si) parameter.

4. CORDIC BASED HIGH PASS FIR FILTER

We have chosen an arbitrary frequency response equation of a High Pass FIR filter [12] is given by equation.

$H(e^{jw}) = 0.75 - 0.45\cos w - 0.31\cos 2w - 0.15\cos 3w$

In this paper we have find out the magnitude value and response of the filter. By using the CORDIC algorithm find out the cosine value of the given angle. And then by using adder and sub-tractor find out the magnitude value.

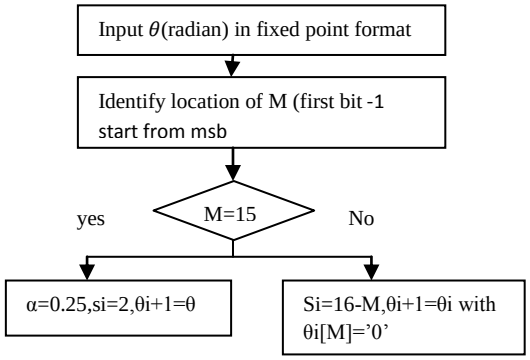

Fig 1: Flow Chart for Scale Free CORDIC Algorithm

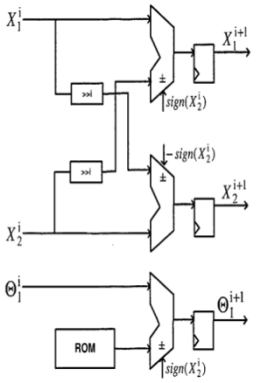

Fig 2: Folded Architecture

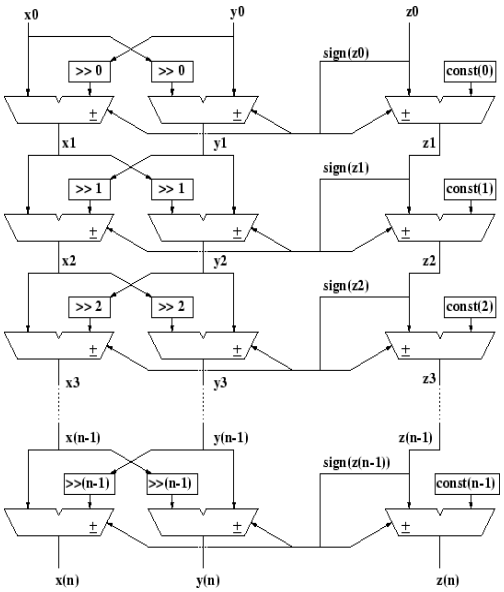

Fig 3: Unfolded Architecture

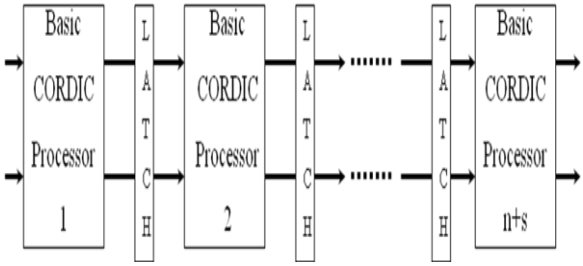

Fig 4: Pipelined Architecture

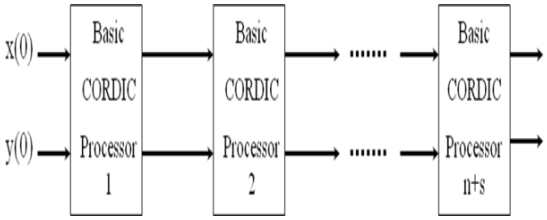

Fig 5: Parallel Architecture

5. RESULTS

(a)Sine cosine Generator by using typical CORDIC Algorithm

x[15:0]= 9945(dec)
1=2^14=16384
x[15:0]=0.607=9945
y[15:0]=0=0
z[15:0]=10(dec)=10degree
x(output)=cos(10°)=0.98(actual value)
Obtained value= 16163(dec)
16163/16384= 0.98
Percentage Error in cos value
= (Actual Value-Obtained Value/Actual Value)*100
= (0.98-0.98)*100/0.98=0%.
y(output)=sin (10°)=0.174(actual value)
Obtained value=2644(dec)

2644/16384=0.161
Percentage Error in sin Value= (0.174-0.161)*100/0.174=7.47%
Timing Summary- (Virtex-4) Speed Grade: -12
Minimum period: 30.988ns (Maximum Frequency: 32.271MHz)
Minimum input arrival time before clock: 37.546ns
Maximum output required time after clock: 35.760ns
Maximum combinational path delay: 46.598ns

(b) High Pass FIR Filter designing by using typical CORDIC Algorithm

At angle θ°=10,
H (e^{jw}) = -1893(dec) - obtained value
= -1893/16384=- 0.11
Actual Value= - 0.109.
Percentage Error in Filter output value
= (Actual Value-Obtained Value/Actual Value)*100
= (-0.109+0.11)*100/0.109=0.009%.
In this design we obtained the results for angles from 0° to 29°.
Timing Summary-(Virtex-4) Speed Grade: -12
Minimum period: 32.639ns (Maximum Frequency: 30.638MHz)
Minimum input arrival time before clock: 41.321ns
Maximum output required time after clock: 95.742ns
Maximum combinational path delay: 102.875ns

(c)Sine cosine Generator by using Scale free CORDIC Algorithm

Angle 35°= 9c61 (hex) =40033(dec)
x(output)=cos(35°)=3463(hex)=13411(dec)
=0.81854(obtained value)
Actual Value=cos(35°)=0.891.
Percentage Error in cos value =
(0.891-0.81854)*100/0.891=8.13%
y(output)=sin(35°)=24c6(hex)=9414(dec)
=0.5745(obtained value)
Actual Value= sin(35°)=0.5735.
Percentage Error in sin value= (0.5735-0.5745)*100/0.5735
=-0.17%
Timing Summary-(Virtex-4) Speed Grade: -12
Minimum period: 10.849ns (Maximum Frequency: 92.178MHz)
Minimum input arrival time before clock: 5.909ns
Maximum output required time after clock: 3.879ns
Maximum combinational path delay: No path found

(d)High Pass FIR Filter designing by using Scale free CORDIC Algorithm

At angle θ°=10
H (e^{jw}) = -1873(dec) - obtained value
= -1873/16384=- 0.11
Actual Value= - 0.109.
Percentage Error in Filter output value
= (Actual Value-Obtained Value/Actual Value)*100
= (-0.109+0.11)*100/0.109=0.009%.
In this design we obtained the results for angles from 0° to 15°.
Timing Summary (Virtex-4) Speed grade= -12
Minimum period: 11.545ns (Maximum Frequency: 86.618MHz)
Minimum input arrival time before clock: 6.859ns
Maximum output required time after clock: 44.112ns
Maximum combinational path delay: No path found

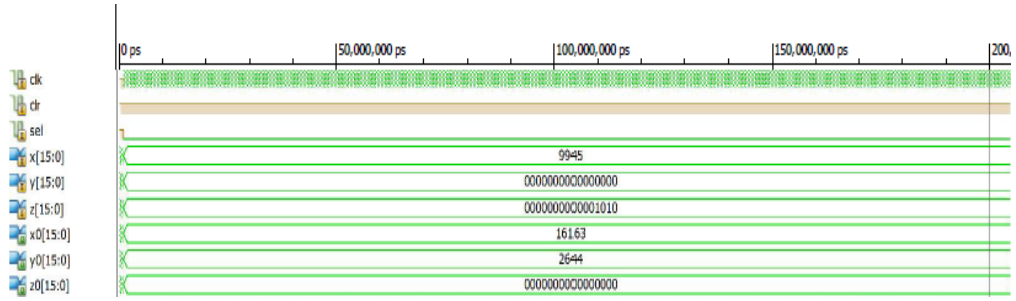

Fig 6: Waveform of the sine cosine generator by using typical CORDIC algorithm

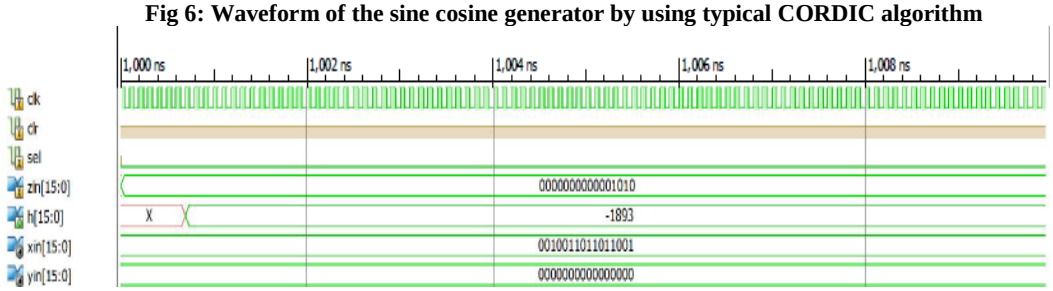

Fig 7: Waveform of the FIR Filter by using typical CORDIC algorithm

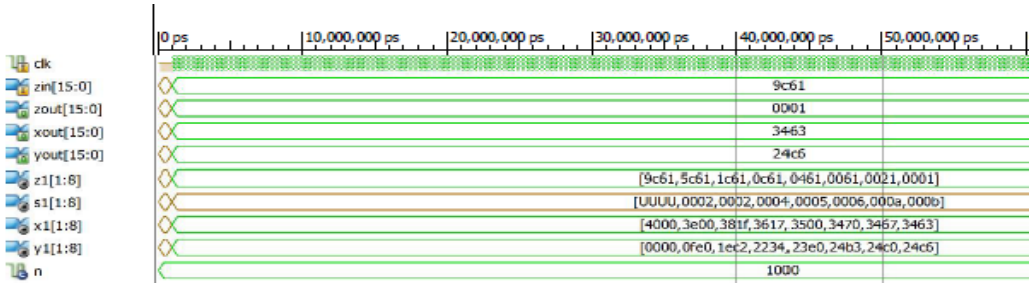

Fig 8: Waveform of the sine cosine generator by using scale free CORDIC algorithm

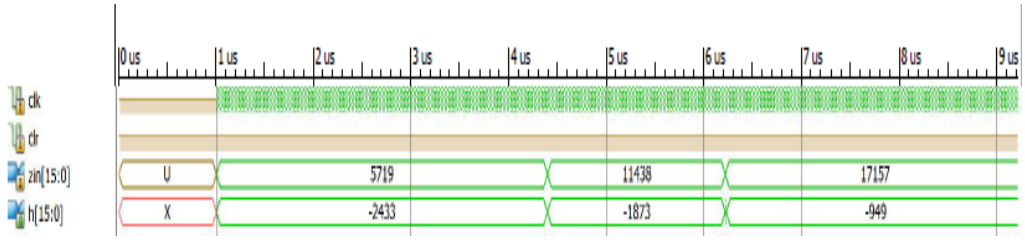

Fig 9: Waveform of sine cosine generator by using scale free CORDIC algorithm

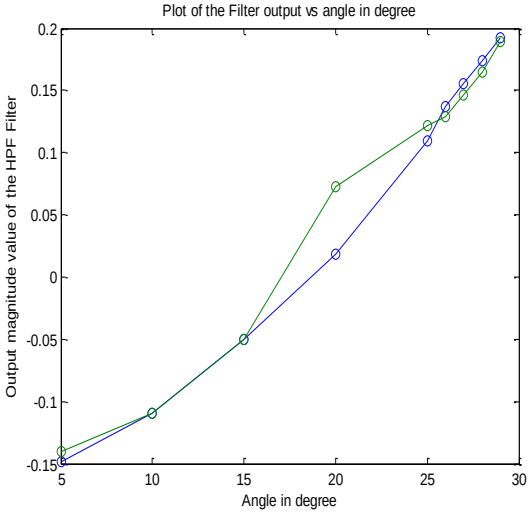

Fig 10(a): Plot of Filter output vs angle in degree (By using typical CORDIC algorithm)

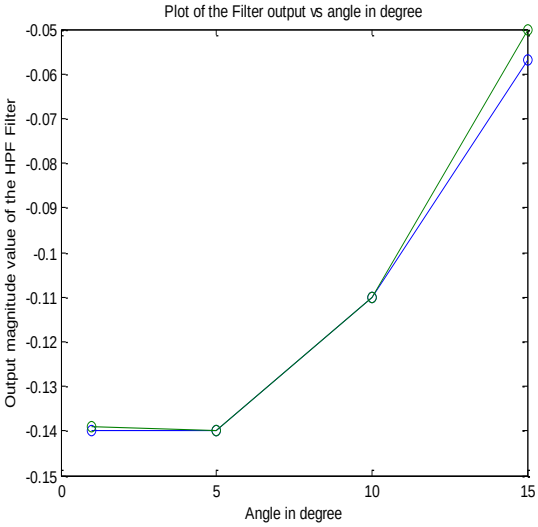

Fig 10(b): Plot of Filter output vs angle in degree (By using scale free CORDIC algorithm)

Table1: Hardware Utilization of Sine cosine generator

Algorithm	Device Parameter	No of Usage	No of Available	Utilization
Typical CORDIC Algorithm	No of Slice Register	168	71,680	1%
	No of Slice LUTs	910	71,680	1%
	No of bonded IOB	99	768	12%
	No of BUFG	1	32	3%
Scale-free CORDIC Algorithm	No of Slice Register	780	71,680	1%
	No of Slice LUTs	3,865	71,680	5%
	No of bonded IOB	65	768	8%
	No of BUFG	1	32	3%

Table2: Hardware Utilization of High Pass FIR Filter

Algorithm	Device Parameter	No of Usage	No of Available	Utilization
Typical CORDIC Algorithm	No of Slice Register	479	71,680	1%
	No of Slice LUTs	3,354	71,680	4%
	No of bonded IOB	27	768	3%
	No of BUFG	1	32	3%
Scale-free CORDIC Algorithm	No of Slice Register	2146	71,680	2%
	No of Slice LUTs	12,143	71,680	16%
	No of bonded IOB	34	768	4%
	No of BUFG	1	32	3%

Table3: Comparison of the designing of sine cosine generator based on typical CORDIC Algorithms and scale free CORDIC Algorithm

	Power Consumption	Frequency	Combinational path delay
Typical CORDIC Algorithm based sine cosine generator	0.850 W	32.271MHz	46.598 ns
Scale free CORDIC Algorithm based sine cosine generator	0.691W	92.178MHz	NIL

Table4: Comparison of the designing of High Pass FIR Filter based on typical CORDIC Algorithms and scale free CORDIC Algorithm

	Power Consumption	Frequency	Combinational path delay
Typical CORDIC Algorithm based sine cosine generator	0.660 W	30.638MHz	102.875 ns
Scale free CORDIC Algorithm based sine cosine generator	0.769W	86.618MHz	NIL

6. CONCLUSION

In these observations we notice that scaling free CORDIC algorithm based two different designs have higher frequency, less time period and low power consumption as compared to typical CORDIC algorithm based designs.

Scaling free CORDIC Algorithm based sine cosine generator and FIR HPF has less (i) input arrival time before clock (ii) output required time after clock (iii) combinational path delay as compared to typical CORDIC algorithm. So the Scaling free CORDIC algorithm gives more advantages than typical CORDIC algorithm.

But the occupied space of scaling free CORDIC algorithm based designs is slightly more than the typical CORDIC algorithm based designs. The typical CORDIC algorithm has the range of target angle for the calculation of sine cosine generator is from 0° to 90°, and for scaling free CORDIC algorithm the range of convergence is from 0° to 45°.So in case of conventional CORDIC algorithm based filter design has the plot of the output magnitude vs angle variation from 0° to 29° and in case of scale free CORDIC algorithm based filter design has the plot of the magnitude vs angle variation from 0° to 15°.The scale free CORDIC algorithm based high pass FIR filter has more closer results to the calculated results as compared to the conventional CORDIC algorithm based high pass FIR filter.

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