FPGA Implementation Content Addressable Memory in Cache Applications

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ABSTRACT
Content Addressable Memory (CAM) is a special type of high speed memory device that can support to compare all the stored data in parallel with a given input data in an efficient way and provide the address of the match data. Read, write, and match are three characteristics of a CAM memory. Read and write are operation of a CAM array in the same way as simple memory. Match mode is the unique operation of the CAM memory. CAM is frequently used in high speed searching operation such as lookup tables, communication networks, pattern recognition, data compression and real signal tracking. The match time of CAM structure is faster and employs better performance than other types of memory. Advancements in VLSI technology FPGAs have high throughput and short time to market make it most attractive in hardware industry. This paper design CAM cell in addition with dual port Synchronous Static Random Access Memory (SSRAM) in cache memory. Hardware realization of this proposed architecture is described using Hardware Description Language (HDL). The operation speed of this proposed module is 306.184MHz in Spartan-6 FPGA platform.

General Terms
Reconfigurable Architecture

Keywords
Content addressable memory (CAM); Cache; FPGA; dual port SSRAM; VHDL;

1. INTRODUCTION
CAM is a special storage device, is also known as associative memory. Traditionally memory store data and return the data by address specific memory locations. It is a lengthy process to search an item and therefore, time consuming is an important factor for fast memory access operation. CAM is the alternative storage device to reduce the access time by searching its content rather than address. CAM stores a large amount data and compares input data against all stored data in parallel in a single clock cycle and return the address of the matched data. CAMs are search engines that are much faster than other searching algorithms like binary or tree-based search etc. CAM is high speed memory applicable in network routers, asynchronous transfer mode (ATM), databases and many more.

The CAM is famous for its high speed searching operation but at the same time it have high power dissipation, low bit density, and at high cost per bit [1]. Designers are trying to optimize the area and power and also improve the speed the system. Unlike RAM requires an address and returns the stored data at that address. But in CAM, data word is provided and then CAM searches its entire memory in it. If the data word is found then the CAM return the address of data word. CAM device are very much expensive compare with other conventional memory systems due to its complex match logic circuit. But advancement in VLSI technology, this CAM become economically feasible and applications employed in such system where data must be accessed very rapidly. Recently, CAM device applications include image processing, artificial intelligence, real time pattern matching.

Many researchers are trying to develop a high capacity CAM device with optimal hardware resource. In [2], the authors proposed implementation of SRAM based ternary CAM. The proposed architecture is low power dissipation with high speed data searching operation. In this paper, authors described CAM implementation for information detection. The authors also designed dual port RAM for implementing CAM circuit on FPGA [3]. FPGA implementation CAM device are highly desirable in hardware industry due to virtue of FPGA technology. FPGAs are flexible devices with low power consumption and compared with application specific integrated circuit (ASIC). The low non- recurring cost and reduce development time make it right choice for implementing CAM on FPGA development board. CAM device is mostly used in address mapping for caches. Small information is quickly retrieved through the CAM structure. Hardware acceleration with FPGA is important in cache application. This paper designs CAM using dual port SSRAM for cache application which will perform read, write and match operation. The designed architecture is designed in VHDL and implement on FPGA. The aim of this paper is to implement a reconfigurable high speed CAM device with optimum resource uses.

This paper describes implementation CAM cell with dual port SSRAM in Cache applications. The CAM cell and dual port SSRAM architectures are codded in VHDL for functional verification, synthesized and then bits stream are download on FPGA board. The rest of the paper is organized as follows: Section 2 describes the CAM in cache application. . Section 3 deal with real time FPGA implementation. Simulation result, RTL schematic, device utilization is also shown in this section. At last, section 4 concludes the paper.

2. CAM IN CACHE APPLICATION
Cache is a high fast intermediate memory device that can store small information out of total memory in a digital system. The cache location is found between the processor

and large secondary memory. Fig. 1 shows the application of CAM cell in cache memory.

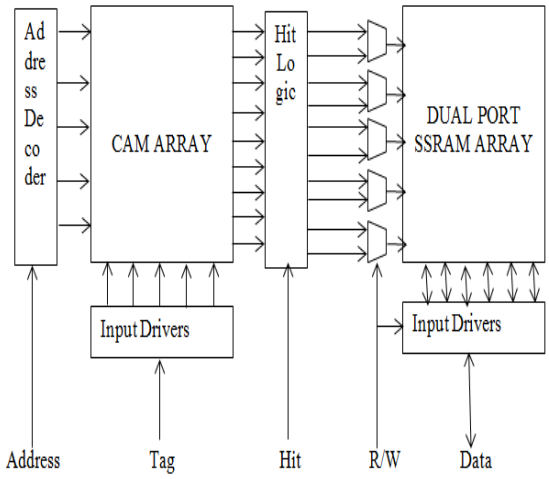

Fig 1: Application of CAM cell in cache memory

The cache memory array consists of two parts, one is the CAM array that can store the address and the other part is dual port SSRAM array which can store data. Dual port memory has separate address decoders and data multiplexers for each access port. Dual port memory circuit area is larger than single port memory with same data storage. But due to fast access time, it is typically used in high speed device. Dual port SSRAM is used for read and write operation. When the processor needs to write data, the address is written into the CAM array and data into the dual port SSRAM array. For a new entry of address and data needs to be written and the cache is full and then one entry should be displaced through cache replacement policy. During read operation, the address of the data requested is obtained to the CAM array and parallel search action is occurred. A match significant the data certainly exists in the cache array. The match signal acts as the word line enable for the dual port SSRAM array which finally delivers the data. For mismatch condition, the data must be obtained from external slow memory system and as a result cache miss has occurred.

3. FPGA IMPLEMENTATION

This section simulation result of hardware modules has been implemented along with its RTL schematics and device utilization. The CAM array and dual port 4K X 8-bit SSRAM has been developed in VHDL code and synthesized. It has implemented on reconfigurable FPGA platform. The functionality has been checked by using Xilinx ISE design suite 14.7. Xilinx Spartan 6 is used for porting the implemented design.

Dual port memory is typically used in high speed network connection. One port allows data is to be written and read, while the other port only allows data is to be read. In dual port model, there is no separate provision for the possibility of parallel read and write accesses to the same address. Fig. 2 shows the simulation wave form of dual port 4K X 8-bit SSRAM

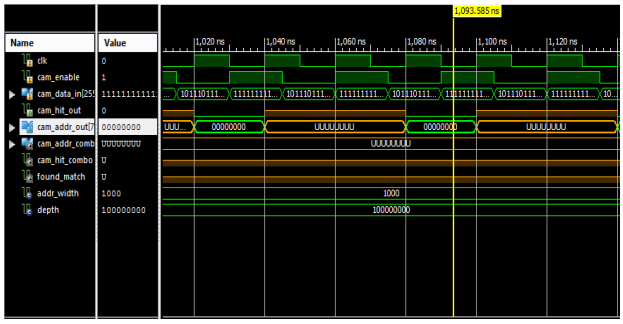

Fig 2: Simulation result of dual port 4K X 8-bit SSRAM.

During simulation, if read_write_port is activated first, it modifies the memory location, and the read operation yields the modified value. On the other part, if read_only_port is activated first, it reads the old value before the location is modified. When the model is synthesized, the synthesis tool takes a dual-port memory component from its library. The effect of a parallel read and write would depend on the behavior of the select component. The RTL schematic is shown in fig. 3.

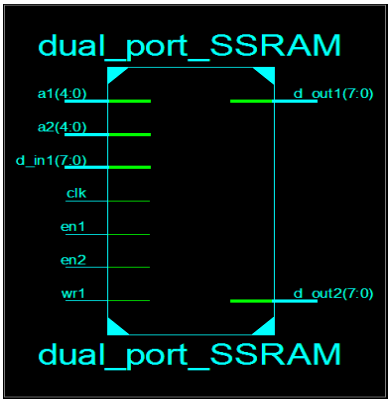

Fig 3: Dual port SSRAM structure

Table 1 shows the estimated hardware resource for dual port SSRAM.

Table 1. Device utilization summary of dual port SSRAM

Synthesis Parameter	Dual port SSRAM
Number Slice Registers	16
Number of Slice LUTs	16
Number used as Flip-Flops	16
Number of IOBs	38
Total memory usage	233768 kilobytes

Fig. 4 shows CAM structure simulation waveform with word size 256 and address 8-bit.

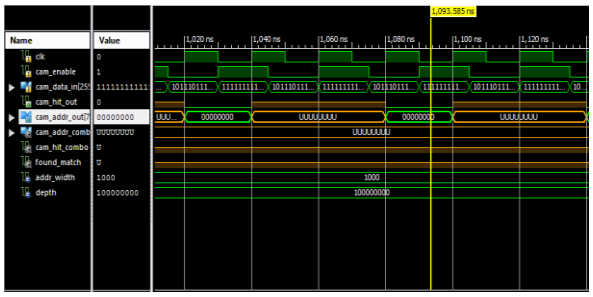

Fig 4: Ssimulation waveform of CAM structure

Fig. 5 shows the RTL schematic of the CAM structure. Input data word length 256-bit and corresponding output address 8-bit width. CAM itself searches entire memory in single clock cycle and CAM device is much faster than other memory system like RAM. If the input cam_data_in matches with stored data in memory then cam_hit_out will be high and provides corresponding match address that is cam_addr_out. A no-match signal identifies a cache miss

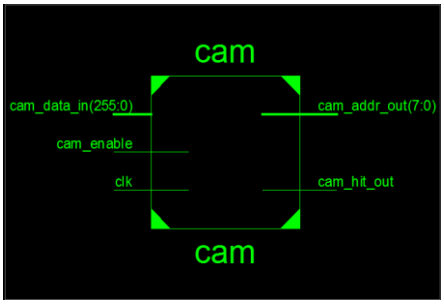

Fig 5: RTL schematic of CAM structure

4. CONCLUSION

In this paper a hardware realization of a CAM cell to a fully associative cache memory is designed and implemented it on FPGA platform. CAM is a special type of memory that can store data, read data and retrieve data. Hardware acceleration with FPGA is important part in CAM cell for searching data-bases, list, images and voice recognition. The presented CAM hardware with dual port SSRAM is flexible and high speed CAM cell is fast memory access with a cost of area. The time required to find an item stored in memory location can be drastically reduced if the item can be search by its content rather than its address. The computation speed of this CAM cell is 306.184MHz.

device. In future, various hardware optimizing technique apply to CAM cell for reduce the hardware cost and also pipeline architecture improve speed of the system.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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