Microprocessor Compatible PWM Generator Implement on FPGA

Bapan Singh, Prashant Kumar Dubey, Arijit Roy
Students, ECE Dept.
Brainware Group of Institutions
Kolkata

Debarshi Datta
Assistant Professor
ECE Dept.
Brainware Group of Institutions
Kolkata

ABSTRACT
This paper is concerned about microprocessor compatible PWM generator architecture by using Field Programmable Gate Array (FPGA). In PWM the variation of duty cycle change the width of the pulse. The PWM generator (PWMG) is interfaced to the bus of a microprocessor. The microprocessor initiates PWMG to specify duty cycle. The duty cycle remain unchanged until new data available to the PWMG from microprocessor unit. The output signal of PWMG is logic "1" and logic "0" for a specific time period. The architecture has been designed with VHDL code and verified using Xilinx ISE Design Suite 14.7. The design is successfully implemented on SPRATAN-6 FPGA board. The operating frequency of this proposed architecture is of 292.650MHz.

Keywords
Duty cycle, Microprocessor, PWM,VHDL, FPGA

1. INTRODUCTION
A pulse width modulated (PWM) signal is widely used in industry like DC-DC converters, motor speed controlling, solar tracking , power converter and many more. The very low power loss in the switching devices is the main advantage of PWM. In switch off mode no current is flowing and in on state, there is zero voltage drop across the switch. The power loss which is calculated by the multiplication of both voltage and current is zero for these cases. The proper adjustment of the duty cycle, the PWM also uses in digital domain where ON/OFF is natural state.

Pulse width modulation is basically variation of pulse with respect to time. The main parameter of PWM is duty cycle which can be varied according the desired value. The duty cycle (D) can be calculated of the following equation

$$D = \frac{T_{ON}}{T} \quad (1)$$

Where $T = T_{ON} + T_{OFF}$

The output signal can be obtained by following equation

Output = (duty cycle) X (input) (2)

The motor speed can be controlled by variation of duty cycle. For very short period of PWM signal, the motor's speed is directly related to the signal's duty cycle. On the other contrary, for very large time period the motor's speed is no longer controlled by the average value of the PWM signal. The motor rotates with high speed for PWM signal 1 and stop for 0 PWM signal. Figure 1 shows pulse width modulated signal with different duty cycles.

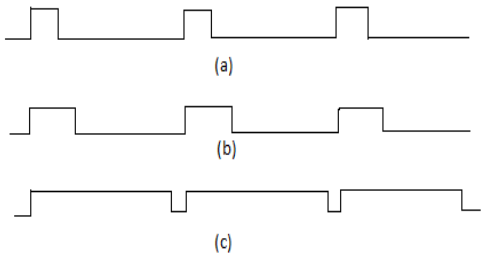

Figure 1. Pulse width modulated waveforms (a) 20% duty cycle (b) 40% duty cycle (c) 90% duty cycle

FPGAs are one of the suitable platforms for realization PWMG. The inherent parallel data stream, optimization, flexibility and short time to market make it very attractive compare to other processor architectures like DSPs, Microcontrollers. FPGA is the portable platform for several real-world applications.

The implementation of PWM in FPGA is an important research area. The PWM controller was implemented on FPGA with high frequency [1]. In [2] the author proposed a hardware-based PWM signal generation for control in motor. In paper [3], the author described generation of PWM signals with variable duty cycle. The model was codded in VHDL with operating frequency 10MHz and tested on FPGA. In paper [4], the authors proposed generation of PWM signals using VHDL based on FPGA. The output of PWM signals have a fixed frequency (11.8 KHz) depended on the frequency of sawtooth, and a variable duty cycle that changes from 0% to 100%.

This paper designed microprocessor compatible PWM signal generation in VHDL and successfully tested on FPGA board.

2. PROPOSED ARCHITECTURE
This section is been designed PWM signal generator (PWMSG) to be interfaced to the bus of a microprocessor. The proposed design is consisted of register and counter with proper data input. The microprocessor writes a data byte to the PWMSG for generating specific duty cycle. The output of

PWMSG duty cycle is unchanged till the microprocessor writes a new data byte to the PWMSG. The block diagram of the proposed system is shown in Figure 2. The microprocessor clock (clk) is used to operate the clock input of the PWMSG. The microprocessor clock frequency is reduced by prescalar

subsystem to generate low frequency signal, ps. This ps signal is applied to the period counter to count the triggering edge of the microprocessor clock. The period counter output (period_cnt) is used for period of PWM signal which is 256 times period of the prescalar output (ps). The period of the PWM output signal, pwm_out, is defined as the time require period_cnt to cycle from 0 through 255 and then roll over to 0. The subsystem duty cycle provides 8-bit duty_cycle. The microprocessor is written on duty cycle subsystem to control the duty_cycle. The microprocessor provides data to duty cycle subsystem and controls the write operation using the cs_bar and we_bar inputs. The value of pwm_out duty cycle is depend upon data input the duty cycle subsystem divided by 256.

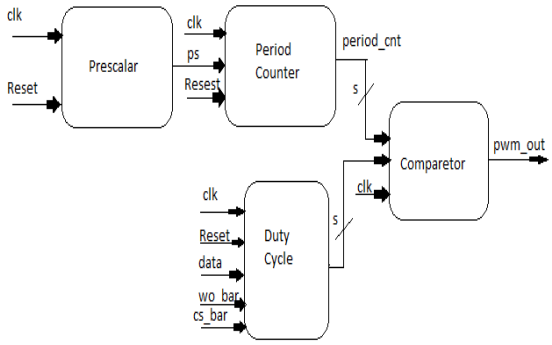

Figure 2. Microprocessor compatible Pulse Width Modulated Signal Generator

For example, to achieve 25% duty cycle the data input from microprocessor is of 64 to duty cycle subsystem. Then comparator compares the output of the period counter period_cnt with the duty_cycle from the duty cycle subsystem. If duty_cycle value is more than period_cnt, then output of the comparator pwm_out '1'; otherwise '0'.

3. FPGA IMPLEMENTATION

This proposed hardware modules has been simulated along with its RTL schematics by Xilinx ISE design suite 14.7 and synthesized bits stream are downloaded on Spartan 6 to target device XC6SLX45. VHDL code for proposed design is given below..

```
entity pwm_micro is
    Port ( data: in std_logic_vector (7 downto 0);
           cs_bar: in std_logic;
           we_bar: in std_logic;
           clk: in std_logic;
           reset: in std_logic;
           pwm_out: out std_logic);
end pwm_micro;

architecture Behavioral of pwm_micro is
signal ps : std_logic;
signal period_cnt : std_logic_vector(7 downto 0);
signal duty_cycle : std_logic_vector(7 downto 0);
begin
prescalar : process (clk)
  variable pscount_v : unsigned(7 downto 0);
  variable ps_v : std_logic;
  begin
if rising_edge(clk) then
  if reset = '1' then
   pscount_v := "10000100";
   ps_v := '0';
   else
    case pscount_v is
     when "00000001" => pscount_v := "10000100";
     ps_v := '1';

      when others =>
      pscount_v := pscount_v - 1;
      ps_v := '0';
      end case;
      end if;
      ps <= ps_v;
      end if;
      end process;
period_cntr: process (clk)
variable count_v : unsigned(7 downto 0);
 begin
 if rising_edge(clk) then
if reset = '1' then
count_v := (others => '0');
 elsif ps = '1' then
 count_v := count_v + 1;
 end if;
 period_cnt <= std_logic_vector(count_v);
 end if;
 end process;
duty : process (clk)
begin
if rising_edge(clk) then
if reset = '1' then
duty_cycle <= (others => '0');
 elsif we_bar = '0' and cs_bar = '0' then
 duty_cycle <= data;
 end if;
 end if;
 end process;
comparator : process (clk)
begin
if rising_edge(clk) then
 if reset = '1' then pwm_out <= '0';
 elsif period_cnt < duty_cycle then pwm_out <= '1';
 else pwm_out <= '0';
 end if;
 end if;
 end process;
end Behavioral;
```

The simulated waveform is shown in Figure 3.

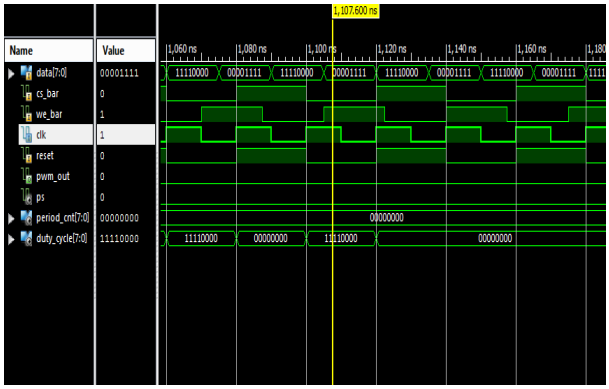

Fig 3: PWMG Timing waveform

The RTL schematic of the PWMSG is shown in Figure 4.

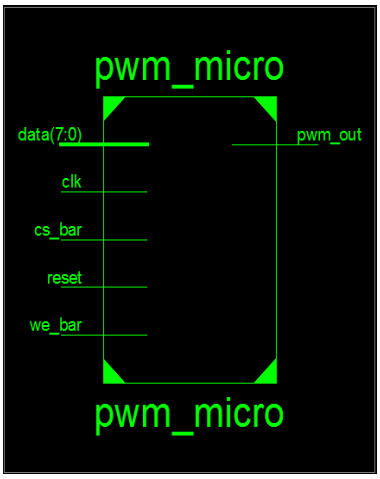

Fig 4: RTL Schematic of PWMG

The hardware resources like slice registers, LUTs, flip-flops are described in table 1. The operating speed of this PWMSG is of 292.650MHz.

Table Error! No sequence specified.. Device utilization summary of PWMG

Synthesis Parameter	PWM Generator
Number Slice Registers	26
Number of Slice LUTs	24
Number used as Flip-Flops	26
Number used as logic	23
Number of IOBs	13

4. CONCLUSION

In this paper, FPGA based microprocessor compatible PWM signal generation is discussed. Microprocessor writes data into PWMG to produce particular duty cycle. Microprocessor controls the PWMG for providing variation pulse width. The system has been designed in VHDL and functional verification is obtained from Xilinx ISE 14.7 simulator. The synthesized bit stream is downloaded on Spartan-6 FPGA board to yield hardware resources and computation time. The experimental result shows that proposed designed occupy less number of slices which represent the area of PWMG. The operating frequency of the PWMG is of 292.650MHz which leads to fastest operation. The output of the PWM signal is applicable to DC-DC converter, motor, robot and many other applications.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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