Abstract

Increasing Processing capabilities of graphic devices and recent improvements in CCD technology have made hexagonal sampling attractive for practical applications. Also, hexagonal representation has special computational features that are pertinent to the vision process. This paper describes Edge detection operation on hexagonally sampled images and its hardware implementation based on Cellular Logic Array Processing (CLAP) algorithm. This architecture
builds up a virtual hexagonal grid system on the memory space of computer and processing algorithms can be implemented on such virtual spiral space, thereby decreasing the computational complexity. These operations were done on hexagonal sampled grid using MATLAB version 7 and the results were compared with rectangular sampled grid. MODELSIM and Quartus II software were used for analysis and synthesis. The performance was tested using Altera Cyclone II FPGA. It was observed from the results that there is a marginal improvement while processing with hexagonal sampled grid. Hardware utilization is found to be less for the image sampled on hexagonal grid compared with rectangular grid.

Reference

- Laurent Condat and Van De Ville, “Quasi-Interpolating Spline Models for Hexagonally-Sampled Data,” IEEE Transactions on Image Processing, vol. 16, No. 5,
Hardware Implementation of Edge detection on Hexagonal Sampled Image Grids

- Muthkumar Venkatesan and Dagggu Venkateshwar Rao,“ Hardware Acceleration of Edge Detection Algorithm on FPGAs. www.celoxica.com/cup/papers

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CLAP algorithm
FPGA implementation of CLAP algorithm