Abstract

Vedic multiplier is based on the ancient algorithms (sutras) followed in INDIA for multiplication. This work is based on one of the sutras called "Nikhilam Sutra". These sutras are meant for faster mental calculation. Though faster when implemented in hardware, it consumes more power than the conventional ones. This paper presents a technique to modify the architecture of the Vedic multiplier by using some existing methods in order to reduce power. The 32 X 32 Vedic multiplier is coded in Verilog HDL and Synthesized using Synopsys Design Compiler. The performance is compared in terms of area, data arrival time and power with earlier existing architecture of Vedic multiplier. The proposed design shows very good improvements in terms of power.

References

- C. R Baugh and B. A Wooley, "A Two's Complement Parallel Array
Implementation of Power Efficient Vedic Multiplier


Index Terms

Computer Science
Algorithms

Keywords

Vedic Multiplier Low Power Multiplier Nikhilam Sutra