This paper presents a high-speed and low area 16 x16 bit Modified Booth Multiplier (MBM) by using Carry Select Adder (CSA) and 3-stage pipelining technique. CSA improves the performance of MBM and pipelining technique reduces the delay time. Using these techniques, the delay is reduced by 56% and the numbers of SLICES and LUT's are reduced by 4% as compared to high speed MBM. The multiplier circuit is designed using VHDL and simulated using Xilinx ISE Simulator. The power metric of the MBM is evaluated using Cadence tools.

References


**Index Terms**

Computer Science

**Keywords**

Carry Select Adder (CSA)  Pipelining  Modified Booth Multiplier  Xilinx Isim  Cadence