Abstract

This paper proposes that several FFT algorithms such as radix-2, radix-4 and split radix were designed using VHDL with the multiplication complexity reduced more than 30% by using the newly proposed CSD constant multipliers instead of the programmable multipliers and the simulations of standard 0.35 μm. The sizes of FFT/IFFT operations are varied in different applications of OFDM systems. The reorganized Mixed Radix 4-2 Butterfly FFT with bit reversal for the output sequence derived by index decomposition execution is our suggested VLSI system architecture to design the module FFT/IFFT processor for OFDM systems. The output shows that the proposed processor architecture can minimize the area cost while keeping a high-speed processing speed, a decrement of more than 70% of the power consumption/area when compared with complex multiplier.

References

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- "A High-Speed Low-Complexity Modified FFT Processor for High Rate WPAN Applications" Very Large Scale Integration (VLSI) Systems, IEEE Transactions on volu pp,Issue :99 page no 1-5

**Index Terms**

Computer Science    
Signal Processing

**Keywords**

Fft/iff Fdm Radix24 Radix22 Multiplier