Abstract

The increasing complexity of software is incessant, this phenomenon is even more accentuated when temporal aspects are introduced, hence the need for rigorous verification methods. The main purpose of this paper is to propose a quantitative verification approach based on model checking. Their properties are expressed in TCTL (Timed Computation Tree Logic) on real-time systems. The system behavior is expressed by temporal labeled systems; namely Durational Action Timed Automata model (DATA* model). This model supports the expression of the parallel behavior, the temporal and structural non-atomicity of actions and urgency. Our approach is to interpret the behavior described by DATA* to Timed Safety Automata. The environment UPPAAL allows us verifying quantitative temporal properties, especially the bounded liveness.

References

Number 11

pages 322–335.

(VECoS'2008), University of Leeds, UK. BCS.

**Index Terms**

Computer Science  
Information Sciences

**Keywords**

Formal verification  
Model Checking  
TCTL  
DATA*s model  
Timed Safety  
Automata  
Bounded Liveliness  
UPPAAL