Abstract

The Analog to Digital converters (ADC) play a very important role in today’s world of electronic systems. The requirement of present applications demands high speed, low power dissipation, minimum area, low noise and application specific resolution. Out of the various types of ADCs available the flash ADC is most popular for its highest conversion rate and its wide applications. On the down side the flash ADC dissipates high power due to the presence of resistance ladder. The power dissipation further increases with increase in resolution. In this research two different approaches are presented which eliminates the resistor ladder completely and hence reduce the power demand drastically. The first approach is Switched Inverter Scheme (SIS) ADC; it is realized for 3 bits using 7 comparator circuits of varying size in CMOS 45nm technology with Predictive Technology Model (PTM). The test result obtained indicates an offset error of 0.014 LSB. The full scale error is of -0.112LSB. The gain error is of 0.07 LSB, actual full scale range of 0.49V, worst case DNL & INL each of -0.3V. The power dissipation for the SIS ADC is 207.987 µwatts; Power delay product (PDP) is 415.9 fWs, and the area overhead is 1.89µm². The second approach is Sleep transistor SIS ADC. This approach shows 71% improvement in power dissipation. Whereas PDP is found to be 107.3 fWs and area overhead is 1.94 µm² for Sleep transistor SIS ADC.
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Index Terms
Keywords

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sleep transistor