Abstract

Reconfigurable devices, such as Field Programmable Gate Arrays (FPGAs), are very popular in today’s embedded systems design due to their low-cost, high-performance and flexibility. Partially Runtime-Reconfigurable (PRTR) FPGAs allow hardware tasks to be placed and removed dynamically at runtime. A novel 2D area fragmentation metric that takes into account feasibility of placement of future task arrivals is presented. Simulation experiments indicate that proposed technique yield better results than existing fragmentation estimation techniques when used in fragmentation aware placement.

References


**Index Terms**

Computer Science  
Embedded Systems

**Keywords**

Fragmentation  
Partially Reconfigurable FPGA