Abstract

The paper discusses a comparative study of full adders with various logic style of designing. Logic style affects the switching capacitance, transition activity, short circuit current and delay. Various logic styles have been compared taking full adder as a reference circuit and power dissipation and delay as reference parameters. Simulation results of all the full adders at technologies of 180nm, 90nm, 45nm of CMOS process have been provided. It is observed that less power is consumed in the Transmission based full adder than the Convention full adder and Pass Transistor full adder.
An Efficient Full Adder Design using Different Logic Styles

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Index Terms

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Keywords

CPL Complementary CMOS DPL Transmission Gate (TG) Pass Transistor Logic Adder

Circuits Low Power Logic Styles.