Effect of underlap on 30 nm Gate Length FinFET based LNA using TCAD Simulations

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ABSTRACT
The effect of gate – drain/source underlap (Lun) on a narrow band LNA performance has been studied, in 30 nm FinFET using device and mixed mode simulations. Studies are done by maintaining and not maintaining the leakage current (Ioff) of the various devices. LNA circuit with two transistors in a cascode arrangement is constructed and the input impedance, gain and noise-figure have been used as performance metrics. To get the better noise performance and gain, Lun in the range of 3-5 nm is recommended.

Keywords
FinFET; LNA; TCAD; Underlap

1. INTRODUCTION
Scaling of CMOS technology not only promises gigabit integration, gigahertz clock rate, and systems on a chip, but also arouses great expectations for CMOS RF circuits in gigahertz range [1]. Drain induced barrier lowering (DIBL) and Short channel effects (SCE) are becoming the fundamental limiting factors in scaling of a single gate planar CMOS transistor. FinFETs are emerging as a potential alternative to MOSFETs due to their quasi planar structure and compatibility with CMOS technology. FinFET, a recently reported novel double-gate structure, the Si fin forms the channel and gate wraps around the fin. The Si fin has insulator on top and gate on either side, current flows parallel to the device surface.

A low noise amplifier (LNA) is a key component in RF front-end receivers which poses a major challenge in terms of meeting high gain and low noise figure at low power supply voltages. In this paper, a FinFET based LNA has been designed and the effect of underlap (Lun) on LNA parameters such as input impedance (Zin), gain (S21) and noise figure (NF) have been studied. This paper presents a LNA design using 30 nm FinFET and the effect of underlap on LNA performance. In the next section, TCAD simulator and the simulation methodology have been discussed. Simulation results are discussed in the section 3. Finally, section 4 gives the conclusion.

2. SIMULATOR AND SIMULATION METHODOLOGIES
2.1 Simulator
Sentaurus TCAD simulator from Synopsys is used to perform all the simulations. This simulator has many modules and the following are used in this study.

- Sentaurus structure editor (SDE): To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation
- Sentaurus device simulator (SDEVICE): To perform all DC, AC and noise simulations
- Inspect and Tecplot: To view the results.

Mixed mode simulation facility of SDEVICE is used to investigate the performance of LNA. The physics section of SDEVICE includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. Noise models such as diffusion noise, monopolar generation-recombination noise, bulk flicker noise are included while doing noise simulations. The structure generated from SDE is shown in Fig. 1. Doping and mesh information can also be observed in Fig. 1. Fig. 2 shows the schematic diagram of the device. The various parameters of the device can be seen in Fig. 2. Table 1 gives the dimensions of the typical device used in this study.

![Figure 1. Structure generated from TCAD](image-url)
Table 1. Typical device dimensions

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Length</td>
<td>30 nm</td>
</tr>
<tr>
<td>Fin Width</td>
<td>5 nm</td>
</tr>
<tr>
<td>Source width</td>
<td>15 nm</td>
</tr>
<tr>
<td>Source length</td>
<td>15 nm</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>2 nm</td>
</tr>
</tbody>
</table>

2.2 Simulation methodologies

The LNA circuit used in this study is shown in Fig. 3. Generally, a common source LNA is used with a source degeneration inductor to get the impedance match, especially to get the real part of input impedance. But, this circuit does not use any source inductor. Instead, it exploits the non-quasi-static (NQS) effects or the channel resistance which arises due to finite charging time of the channel carriers to get the impedance match [2]. An input impedance of 50 Ω, purely resistive, is desired for LNA. The imaginary part i.e. the capacitive part of the input impedance is cancelled at the given frequency, by connecting an appropriate inductor at the gate (L_g). SDEVICE simulator is used for mixed mode simulation of LNA circuit (Fig. 3). Transistors M1 and M2 are simulated at the device level. Other elements are simulated using the compact models at the circuit level. M1 and M2 are identical transistors. Inductors L_g and L_o are used with their series resistance incorporated, and a quality factor of 5 is assumed. Resistances associated with the inductors are given by the following familiar expression,

\[
R = \frac{2\pi f \text{ inductor value}}{\text{quality factor}}
\]

(1)

The circuit is operated at the supply voltage of V_{dd} = 1 V, V_{gs} of M1 = 0.5 V and L_o = 1.5nH. The operating frequency (f) of LNA is taken as 10 GHz.

For a two port network NF is defined as [3], [4],

\[
NF = 1 + \frac{1}{S_{11}^S} \left( S_{11}^{gg} + \left| \alpha \right|^2 S_{dd}^{dd} - 2 \text{Re}(\alpha S_{dg}^{ddg}) \right)
\]

(2)

With

\[
\alpha = \frac{Y_{g} + Y_{11}}{Y_{21}}
\]

(3)

Where S_{11}^{S} is the current noise spectrum of the noisy source admittance and is given by,

\[
S_{11}^{S} = 4k_B T \text{Re}(Y_{S})
\]

(4)
\( S_{Ig}^{gg} \) and \( S_{Id}^{dl} \) are the current noise spectrums, at the gate and drain terminals respectively, \( S_{Id}^{dl} \) is the cross-correlation noise spectra between the drain and gate terminals, \( Y_{11} \) and \( Y_{21} \) are the respective admittance (Y) parameters.

When the underlap is changed, the effect is reflected in the device level (\( I_{\text{off}}, I_{\text{on}}, V_{\text{th}}, g_m, f_t \), etc.) as well as in the circuit level (LNA performance metrics such as input impedance, gain, and noise figure). Therefore, two case studies are constructed and LNA performance is studied.

- Case 1: Underlap is changed and \( I_{\text{off}} \) not maintained
- Case 2: Underlap is changed and \( I_{\text{off}} \) maintained

3. RESULTS AND DISCUSSION

Fig. 4 shows the variation in the leakage current (\( I_{\text{off}} \)) and drain current (\( I_{\text{on}} \)) of the 30 nm FinFET with the different \( L_{\text{un}} \) values. As \( L_{\text{un}} \) is increased, the series resistance associated with the channel increases thereby reducing \( I_{\text{off}} \) and \( I_{\text{on}} \) which can be observed in Fig. 4.

\[
Z_m = R_{g} + R_g + r_i
\]

where \( R_{g} \) is the resistance due to gate inductor, \( R_g \) is the intrinsic gate resistance, and \( r_i \) is due to NQS effect. If we assume proper layout technique have been adopted \( R_g \) can be ignored. Since \( r_i \) increases with \( L_{\text{un}} \) [5], the real part of the input impedance increases with \( L_{\text{un}} \). \( C_{\text{eff}} \) in DGMOS can be expressed as [6],

\[
C_{\text{eff}} = \text{Series}(C_{ox}, C_{si}) || C_{ov} || C_{fringing}
\]

where \( C_{ox} \) is the oxide capacitance, \( C_{si} \) is the silicon body capacitance, \( C_{ov} \) is the gate to source/drain overlap capacitance and \( C_{fringing} \) is the fringing capacitance. In our device \( C_{ov} = 0 \),

\[
C_{fringing} = \frac{k \varepsilon_{di} W}{\pi} \ln \left( \frac{\pi W}{\sqrt{L_{\text{un}}^2 + T_{ox}^2}} \right) e^{-\frac{|L_{\text{un}}^2 - T_{ox}^2|}{L_{\text{un}}^2 + T_{ox}^2}}
\]

For the given transistor width (W), as per (7), when \( L_{\text{un}} \) increases, \( C_{fringing} \) decreases, which in turn decreases the \( C_{eff} \) with the increased capacitive reactance. So the imaginary part of the input impedance increases with \( L_{\text{un}} \).

Case 1

It has been seen that the change in \( L_{\text{un}} \) affects the input impedance. When \( L_{\text{un}} \) is changed the input impedance can be matched by adjusting the gate inductor and the width of the transistor. Case 1
focuses on this procedure. The various values of gate inductor and the transistor widths used to match the input impedance to 50 Ω, purely real, are shown in Table 2. Since real part of the input impedance increases with \( L\) (Fig. 5), we need larger transistor widths to achieve 50 Ω, real part. Again it may be recollected from Fig. 5 that \( L\) increases the input capacitive reactance (i.e., imaginary part of input impedance) thereby demanding higher gate inductor values. But it can be noticed from Table 2 that after 4 nm of \( L\), the required gate inductor value decreases. For higher \( L\)’s, larger transistor widths are needed to make real part of the input impedance equal to 50 Ω. But this procedure at some point makes \( C_{\text{eff}}\) to go up i.e. we need smaller gate inductors to cancel out the capacitive reactance. In our simulation, this happens when \( L_{un}=4\) nm (refer Table 2).

### Table 2. Values of \( L_{un}\), \( L_{un}\), \( f_t\), Width and their respective Gain, Noise figure (\( I_{off}\) not maintained)

<table>
<thead>
<tr>
<th>( L_{un}) (nm)</th>
<th>Gate inductor (nH)</th>
<th>( f_t) (GHz)</th>
<th>Width of the transistor (µm)</th>
<th>Gain (( S_{21})) (dB)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>1.35</td>
<td>735.759</td>
<td>16</td>
<td>9.21</td>
<td>1.977</td>
</tr>
<tr>
<td>1</td>
<td>1.55</td>
<td>815.095</td>
<td>17</td>
<td>9.777</td>
<td>1.914</td>
</tr>
<tr>
<td>2</td>
<td>1.75</td>
<td>881.399</td>
<td>19</td>
<td>10.737</td>
<td>1.819</td>
</tr>
<tr>
<td>3</td>
<td>1.9</td>
<td>889.733</td>
<td>20</td>
<td>11.02</td>
<td>1.726</td>
</tr>
<tr>
<td>4</td>
<td>1.95</td>
<td>888.382</td>
<td>21</td>
<td>11.243</td>
<td>1.675</td>
</tr>
<tr>
<td>5</td>
<td>1.9</td>
<td>854.405</td>
<td>22</td>
<td>10.889</td>
<td>1.657</td>
</tr>
<tr>
<td>6</td>
<td>1.7</td>
<td>829.335</td>
<td>24</td>
<td>10.625</td>
<td>1.708</td>
</tr>
<tr>
<td>7</td>
<td>1.55</td>
<td>801.741</td>
<td>25</td>
<td>9.730</td>
<td>1.738</td>
</tr>
</tbody>
</table>

From Fig. 6 it is observed that the gain of the LNA is going through a peak i.e. the gain increases and then decreases with respect to \( L_{un}\). A maximum gain value of 11.243 dB occurs at \( L_{un}=4\) nm. On one hand, the increased transistor width used with increased \( L_{un}\) enhances \( g_m\) and thereby the gain. But on another hand increased \( L_{un}\) increases the series resistance and thereby degrades \( g_m\) at some point which in turn lowers the gain. In essence, for lower values of \( L_{un}\) increase in the transistor width is responsible for increase in \( g_m\) and the decrease in \( C_{\text{ringing}}\) is responsible for the decrease in \( C_{\text{eff}}\). And at higher values of \( L_{un}\), increase in the series resistance is responsible for \( g_m\) degradation and the increase in the transistor width increases \( C_{\text{ringing}}\) which is responsible for the increase in \( C_{\text{eff}}\). From Fig. 6 it can be noticed that NF travels through a minima when \( L_{un}\) is varied. Around \( L_{un}=4\) nm a minimum value of NF is achieved. Let us consider the input stage of Fig. 3. We have a common source amplifier, with an inductor and resistor (includes the parasitic resistance of the inductor) at the gate. Noise-Figure of this stage alone is given by [8],

\[
NF = 1 + \left( \frac{f_o}{f_t} \right)^K
\]  

where \( f_o \) – resonant frequency, \( f_t \) – unity gain frequency, and \( K \) is noise factor scaling coefficient, and depends on the resonant frequency, quality factor of the inductor, ratio \( g_m/ g_{\text{off}}\) (\( g_m\) is

transconductance of the FinFET, \( g_{\text{off}}\) is output conductance of the FinFET at zero drain bias) and process specifications.

![Figure 6.Gain (dB) and Noise Figure (dB) of LNA after getting a 50 Ω input impedance match at 10 GHz, for different underlaps](image-url)
Table 3. Values of $L_{un}$, WF, $f_t$, $L_g$, Width and their respective Gain, Noise figure ($I_{off}$ maintained)

<table>
<thead>
<tr>
<th>$L_{un}$ (nm)</th>
<th>WF (eV)</th>
<th>$f_t$ (GHz)</th>
<th>Gate inductor ($L_g$) (nH)</th>
<th>Width of the transistor ($\mu$m)</th>
<th>Gain ($S_{21}$) (dB)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>4.336</td>
<td>737.26</td>
<td>1.45</td>
<td>16</td>
<td>9.39</td>
<td>1.102</td>
</tr>
<tr>
<td>1</td>
<td>4.334</td>
<td>815.18</td>
<td>1.65</td>
<td>17</td>
<td>9.974</td>
<td>1.045</td>
</tr>
<tr>
<td>2</td>
<td>4.324</td>
<td>866.09</td>
<td>1.9</td>
<td>19</td>
<td>11.04</td>
<td>0.983</td>
</tr>
<tr>
<td>3</td>
<td>4.317</td>
<td>866.21</td>
<td>2.05</td>
<td>20</td>
<td>11.39</td>
<td>0.978</td>
</tr>
<tr>
<td>4</td>
<td>4.312</td>
<td>840.50</td>
<td>2.05</td>
<td>22</td>
<td>12.10</td>
<td>0.962</td>
</tr>
<tr>
<td>5</td>
<td>4.307</td>
<td>812.30</td>
<td>2.05</td>
<td>23</td>
<td>11.83</td>
<td>0.993</td>
</tr>
<tr>
<td>6</td>
<td>4.304</td>
<td>773.54</td>
<td>1.95</td>
<td>24</td>
<td>11.22</td>
<td>1.026</td>
</tr>
<tr>
<td>7</td>
<td>4.301</td>
<td>737.29</td>
<td>1.75</td>
<td>26</td>
<td>10.60</td>
<td>1.071</td>
</tr>
</tbody>
</table>

4. CONCLUSION
In this paper, we have investigated the effect of $L_{un}$ on gain and NF of a 10 GHz, narrow band LNA using TCAD simulations. Changing $L_{un}$ was followed by two philosophies, not maintaining $I_{off}$ and maintaining $I_{off}$. When $I_{off}$ was not maintained, a maximum gain of 11.243 dB was achieved at $L_{un}=4$ nm and a minimum NF of 1.657 dB was achieved at $L_{un}=5$ nm. When $I_{off}$ was maintained around 50 nA, a maximum gain of 12.105 dB and a minimum NF of 0.962 dB was achieved at $L_{un}=4$ nm. $L_{un}$ in the range of 3-5 nm will give optimum gain and NF for this LNA design.

5. ACKNOWLEDGEMENT
This work is supported by Department of Science and Technology, Government of India, under SERC scheme.

6. REFERENCES