Comparative Analysis of 4-bit CMOS Multipliers

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ABSTRACT
A fast and energy-efficient multiplier is always needed in electronics industry especially digital signal processing (DSP), image processing and arithmetic units in microprocessors. Multiplier is such an important element which contributes substantially to the total power consumption of the system. Multipliers of various bit-widths are frequently required in VLSI from processors to application specific integrated circuits (ASICs). Recently reported logic style comparisons based on full-adder circuits claimed complementary pass transistor logic (CPL) to be much more power-efficient than complementary CMOS. However, new comparisons performed on more efficient CMOS circuit realizations and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products. The most important and widely accepted metrics for measuring the quality of multiplier designs propagation delay, power dissipation and area. This paper describes the comparative performance of 4-bit multipliers designed using TANNER EDA, using different logic design styles.

Keywords: Multiplier, CMOS Logic Design Style.

1. INTRODUCTION
The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level [1]. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the attention of the scientific community associated with VLSI design. In recent years, the growth of personal computing devices (portable computers and real time audio and video based multimedia applications) and wireless communication systems has made power dissipation a most critical design parameter [1]. In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product. In multiplication, reliability is strongly affected by power consumption. Usually, high power dissipation implies high temperature operation, which, in turn, has a tendency to induce several failure mechanisms in the system.

Power dissipation is the most critical parameter for portability & mobility and it is classified in to dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized in equation (1) [2]:

$$\begin{aligned} P_{avg} &= P_{switching} + P_{short-circuit} + P_{leakage} \\ &= \left(\alpha_{0\to1} \times C_L \times V_{dd}^{\,2} \times f_{clk}\right) + \left(I_{sc} \times V_{dd}\right) + \left(I_{leakage} \times V_{dd}\right) \end{aligned} \quad (1)$$

The first term represents the switching component of power, where C_L is the load capacitance, f_{clk} is the clock frequency and α is the probability that a power consuming transition occurs (the activity factor). The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$ which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of V_{dd} emerges as a very effective means of limiting the power consumption. However, the saving in power dissipation comes at a significant cost in terms of increased circuit delay. Since the exact analysis of propagation delay is quite complex, a simple first order derivation [3] can be used to show the relation between power supply and delay time

$$T_D \propto \frac{C_L V_{DD}}{K(V_{DD} - V_{TH})^{\alpha}} \quad (2)$$

K - Transistor's aspect ratio (W /L)

V_{TH} - Transistor threshold voltage

α - Velocity saturation index which varies between 1 and 2

Unfortunately, reducing the supply voltage reduces power, but when the supply voltage is near to threshold voltage (from equation 2), the delay increases drastically [4].

Section II gives a short introduction to the most important existing static logic styles and compares them qualitatively. Section III gives the two important multiplier architectures, designed in this paper. Results of quantitative comparisons based on simulations

of different multiplier architectures by using different logic design styles are given in Section IV. Some conclusions and references are finally drawn in Section V and VI respectively.

2. LOGIC DESIGN STYLES

Bisdounis et al. has proposed a large number of CMOS logic design styles [5]. For multiplication, adder is used as a basic element. For arithmetic applications, following three different logic styles are used for a full adder design to achieve best performance results for multiplier design [6].

2.1 Conventional Static CMOS Logic-CSL

The recent VLSI arithmetic applications [6] i.e 4-bit RCA, uses conventional static CMOS logic. The schematic diagram of a conventional static CMOS full adder cell is illustrated in figure 1.

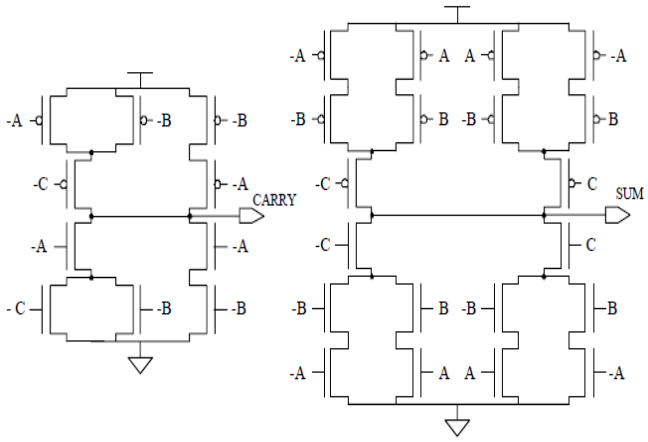

Fig 1: CSL Logic Full adder

The signals noted with '-' are the complementary signals. The p-MOSFET network of each stage is the dual network of the n-MOSFET. Advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing (high noise margins) and thus reliable operation at low voltages and arbitrary (even minimal) transistor sizes (ratio less logic).

2.2 Complementary Pass-transistor Logic-CPL

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used.

CPL [7] uses only an n-MOSFET network for the implementation of logic functions, thus resulting in low input capacitance and high-speed operation [8]. The schematic diagram of the CPL full adder circuit is shown in figure 2. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs [9]. The advantages [10] of pass logic transistors include - Smaller number of transistors and smaller input loads, along with MUX and especially XOR circuits being implemented efficiently. The disadvantage [10] of pass transistor logic is that threshold voltage drops through the NMOS transistors makes it necessary to maintain output voltage level; hence inverter is used at output which increases the number of transistors.

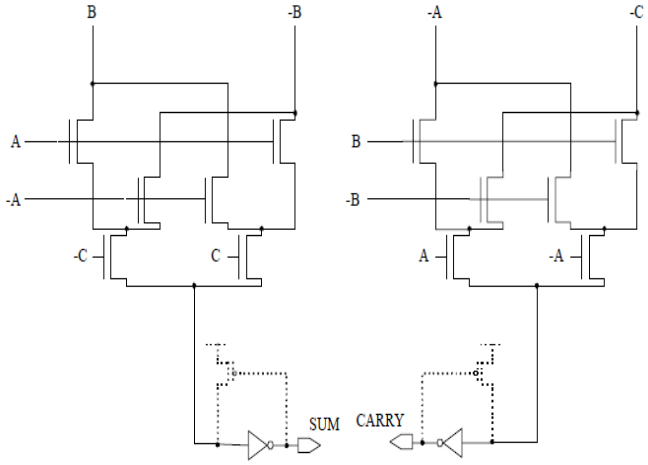

Fig 2: CPL Logic Full adder

2.3 Double Pass-transistor Logic- DPL

DPL [11][12] is a modified version of CPL. The circuit diagram of the DPL full adder is given in figure 3. In DPL circuit full-swing operation is achieved by simply adding p-MOSFET transistors in parallel with the n-MOSFET transistors. Hence, the problems of noise margin and speed degradation at reduced supply voltages, which are caused in CPL circuits due to the reduced high voltage level, are avoided.

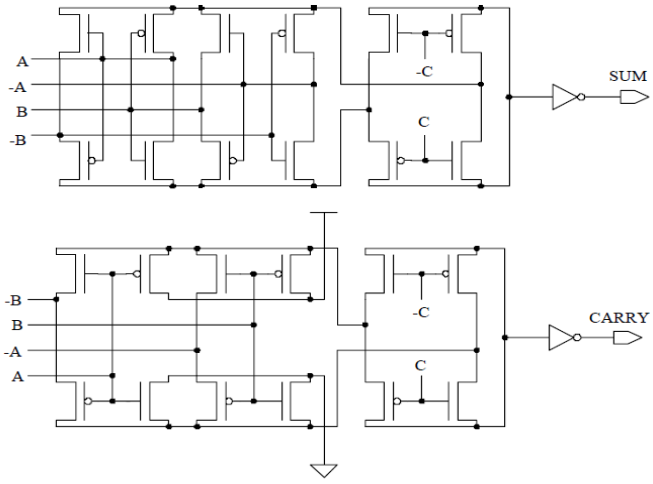

Fig 3: DPL Logic Full adder

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used. However, the threshold voltage drop $(V_{out} = V_{dd} - V_{tn})$ through the NMOS transistors while passing logic "1" makes swing (or level)

restoration at the gate outputs necessary in order to avoid static currents at the subsequent output inverters or logic gates.

3. MULTIPLIER ARCHITECTURES

The wide-bit addition is vital in many applications such as ALUs, multiply-and accumulates (MAC) units in DSPs, and , versatile microprocessor. It is also important for the performance of direct digital frequency synthesizers (DDFSs) where it is used as a phase accumulator. Numerous multiplier implementations exist whereas some are good for low power dissipation and some takes least propagation delay. In multiplication, multiplicand is added to itself a number of times as specified by the multiplier to generate product. In this section, two different 4-bit multiplier architectures are designed.

3.1 Array Multiplier

An array multiplier is very regular in structure as shown in figure 4. It uses short wires that go from one full adder to adjacent full adders horizontally, vertically or diagonally [13]. An n × n array of AND gates can compute all the $a_i b_i$ terms simultaneously. The terms are summed by an array of 'n [n - 2]' full adders and 'n' half adders. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic.

The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders. Each row of full adders or 3:2 compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries.

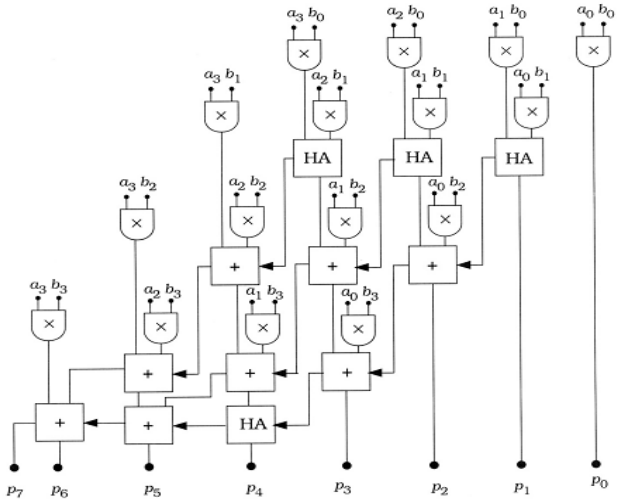

Fig 4: 4-bit Array Multiplier (AM)

The delay associated with the array multiplier is the time taken by the signals to propagate through the AND gates and adders that form the multiplication array. Delay of an array multiplier depends only upon the depth of the array not on the partial product width. The delay of the array multiplier is given by [14]:

$$T(critical) = [(N-1)+(N-2)] * T(Carry) + (N-1) * T(Sum) + T(AND) \quad (3)$$

where $T(Carry)$ is the propagation delay between input and output carry, $T(Sum)$ is the delay between the input carry and sum bit of the full adder, $T(AND)$ is the delay of AND gate, N is the length of multiplier operand.

The advantage of array multiplier is its regular structure. Thus it is easy to layout and has small size. In VLSI designs, the regular structures can be tiled over one another. This reduces the risk of mistakes and also reduces layout design time. This regular layout is widely used in VLSI math co-processors and DSP chips [15].

3.2 Tree Multiplier

C. S. Wallace suggested a fast technique to perform multiplication in 1964 [16]. The amount of hardware required to perform this style of multiplication is large but the delay is near optimal. The delay is proportional to log (N) for column compression multipliers where N is the word length. This architecture is used where speed is the main concern not the layout regularity.

This class of multipliers is based on reduction tree in which different schemes of compression of partial product bits can be implemented. In tree multiplier partial-sum adders are arranged in a treelike fashion, reducing both the critical path and the number of adders needed as shown in the figure 5, shown below:

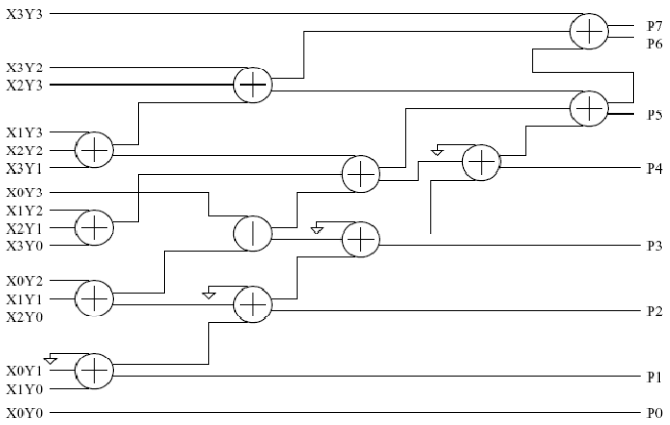

Fig 5: 4-bit Tree Multiplier (TM)

The partial products or multiples are generated simultaneously by using a collection of AND Gates. The multiples are added in combinational partial products reduction tree using carry save adders, which reduces them to two operands for the final addition. The results from CSA are in redundant form. Finally, the redundant result is converted into standard binary output at the bottom by the use of CPA [13].

4. PERFORMANCE PARAMETERS AND SIMULATION SET-UP

The 4-bit multipliers are compared based on the performance parameters like propagation delay, number of transistors and power dissipation. To achieve better performance, the circuits are designed using CMOS process by MOSIS in 0.35μm technology. The channel width of the transistors is 1.7 μm for the NMOS and 4.6 μm for the PMOS. The output capacitance C_L is considered 10fF in all cases whereas the operating frequency is 10 GHz. All the circuits have been designed using TANNER EDA [17]. The

power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention [18]. Direct Simulation method[19] is used in order to analyse the results. The comparative results for two different 4-bit multipliers for different logic design styles are given in Table-1.

Table 1. Performance parameters of 4-bit multipliers

Sr. No.	Multiplier Type	Design Technique	DC Power Dissipation (nW)	Worst Case Propagation Delay (ns)	No. of Transistors	Power Delay Product (n-nJ)
1	Array	CSL	1.01	3.33	432	3.36
		CPL	14.93	1.43	384	21.34
		DPL	10.39	1.82	528	18.90
2	Tree	CSL	0.94	2.85	432	2.67
		CPL	9.11	1.14	388	10.38
		DPL	7.55	1.40	532	10.57

The relationships between various performance parameters of 4-bit multiplier architectures are shown in figure 6.

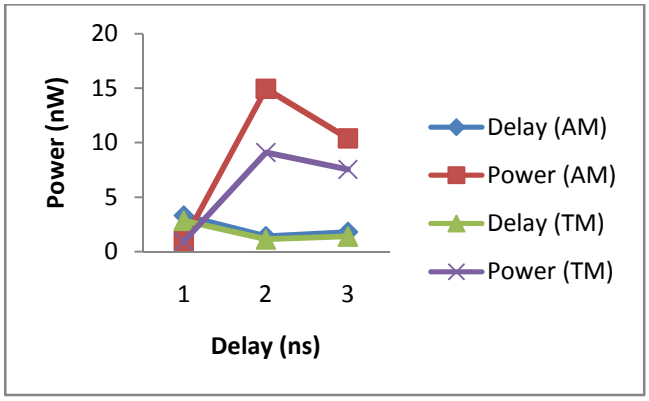

Fig 6: DC Power Dissipation vs Propagation Delay

5. DISCUSSION AND CONCLUSION

It has been observed that complementary pass transistor (CPL) logic design style exhibit better characteristics (speed and area) as compared to other design styles.

So, CPL logic style can be used where portability and high speed is the prime aim. Where, CSL consumes the lowest power among the three. But, the CPL logic design style has propagation delay comparable to DPL and CSL logic design style, so CPL can be considered best logic design style with respect to all parameters of 4-bit multiplier architectures as shown in Table 1.

From the above results, it is observed that array multiplier and tree multiplier exhibits lowest DC power dissipation and comparable propagation delay by using CSL logic design style.

6. ACKNOWLEDGMENTS

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