Ultra Low Power 1-Bit Full Adder

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ABSTRACT
In this paper we propose a new 9 transistor 1-bit full adder. The proposed circuit performs efficiently in subthreshold region to employ in ultra low power applications. The main design objective for this new circuit is low power consumption and full voltage swing at a low supply voltage. The proposed cell also remarkably improves the power consumption, power delay product and has better noise immunity when compared to the existing deigns. All simulations are performed on 45nm standard models on Tanned EDA tool version 12.6.

General Terms
8T and 9T

Keywords
Subthreshold region, full adder and low power.

1. INTRODUCTION
CMOS VLSI circuits have been evolving into low voltage and low power regimes. In recent years VLSI design space has been focusing on high performance microprocessors. Demand for power sensitive, high speed, small area and low cost designs are increasing every day. This tremendous demand is due to fast growth of battery-operated portable applications such as personal computing devices (portable computers and real time audio and video based multimedia products), wireless communication systems (personal digital assistants and mobile phones), medical applications and other portable devices. Broad acceptance of new applications critically depends on the availability of compact and inexpensive hardware delivering the required high performance and longer battery life.. Unfortunately battery capacity has not improved at the same pace as semiconductor performance and integration and it not expected to improve more than 30% every five years. Consequently, integrated circuits (ICs) designed for hand-held applications must increase performance at reduced energy per computation. Also low power designs reduce cooling cost and increases reliability especially for high density systems. This has pursuit the design engineers to develop a much more flexible design to overcome critical issues of low power consuming, small area and efficient designs.

The single-bit full adder is one of the main components in almost all logic structures. The performance of logic structures is highly dependent on the adder cells. The wide use of this operation in arithmetic functions, have made many researchers eager to propose several kinds of different logic styles for implementing 1-bit Full Adder cell, in recent years. To perform arithmetic operation, a device can use up very low power by functioning at very low frequency but it may spend a very long time to finish the operation. The power-delay product can be used for first-level comparison between the different building block designs.

One way to achieve ultra low is by running digital circuits in subthreshold mode [1], [2] and [3]. Subthreshold current of an MOSFET transistor occurs when the gate-to-source voltage (V_{GS}) of a transistor is lower than its threshold voltage (V_{TH}). When V_{GS} is larger than V_{TH}, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as *strong-inversion*, as more minority carriers are present in the channel than majority carriers. When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. In standard CMOS design, this current is a subthreshold parasitic leakage, but if the supply voltage (*VDD*) is lowered below $V_{TH,}$ the circuit can be operated using the subthreshold current with ultra-low power consumption.

The proposed circuit operates efficiently in subthreshold region to achieve ultra low power. The incentive of operating is able to exploit the sub-threshold leakage current as the operating drive current. Results show improvement in threshold loss, speed and power consumption over the other adders with comparable performance. The special feature of this proposed 9T adder is that it has nearly 10 times improved power consumption than its peer design. The rest of the paper has been organized in four sections. Section II briefly describes the previous work existing. We propose the new design of full adder consisting 9T in Section III. Section IV presents the simulation results and finally, Section V concludes the paper.

2. PRIOR WORK
The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, where

Sum = (A **xor** B) **xor** Cin
Cout = A **and** B + Cin (A **xor** B)

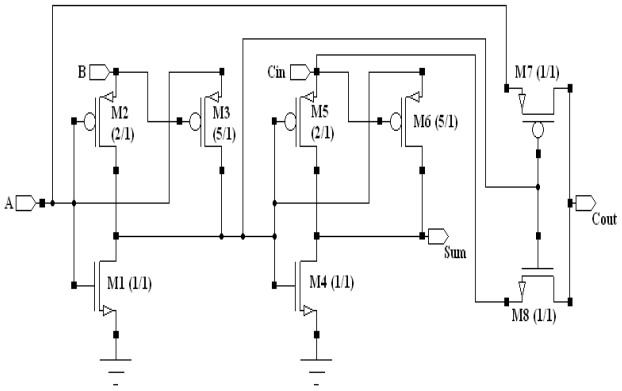

Fig 1: 1-bit 8T Full Adder

Figure 1 shows the circuit of eight transistor 1-bit full adder cell. The Sum output is basically obtained by a cascaded exclusive ORing [4]-[6] of the three inputs. Cout module is implemented using 2T multiplexer. It is quite evident from Figure 1 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain the carry output. The voltage drop due to the threshold loss in transistors M3 and M6 in Figure 1 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of |VT p| provided by the PMOS pass transistor M3 when a=0 and b=0 is used to turn on the NMOS pass transistor M8and therefore we get an output voltage equal to |VTp |-VTn, where VTp is the threshold voltage of the PMOS transistor and VTn is the threshold voltage of the NMOS transistor.

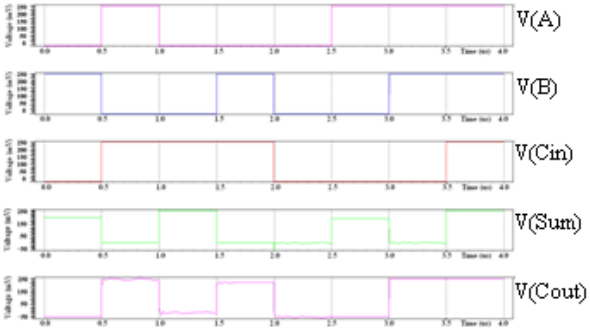

Fig 2: In-out waveform of 1-bit 8T Full Adder

Table 1. Performance of 8T and 9T full adder in terms of Threshold loss

A	B	Cin	Sum(8T)	Sum(9T)
0	0	0	<< $\|V_{tp}\|$	<< $\|V_{tp}\|$
0	0	1	1	1
0	1	0	< 30% of logic "1"	1
0	1	1	0	0
1	0	0	< 30% of logic "1"	1
1	0	1	0	0
1	1	0	<< $\|V_{tp}\|$	<< $\|V_{tp}\|$
1	1	1	1	1

As it can be seen, the 8T full adder Figure 1 is confronted with serious problems especially when Cin=0 and when circuit operates in sub threshold regions. The outputs have good logic level for only a four input vectors. For the remaining input vectors, there is a major degradation in output voltage that may lead to functional failure as well as increased power consumption. As the voltage is scaled down, the signal integrity deteriorates and the speed decreases tremendously.

For input '010', output of the first stage XOR gate is complete '1'. However in the second stage nMOS M4 and pMOS M6 get ON simultaneously. A close loop forms and current feedback through M4 occurs and the output Sum is degraded much less than Vdd (approx. Vdd/2). Similarly for input '100', expected Sum should be '1' and Cout to be '0'. But the first stage XOR gate gives a degraded output less than Vdd (approx. Vdd/2). However at higher input voltages (greater than 0.6v) M1 & M3 and M4 & M6 get ON simultaneously. So, there should be minimum loss at first XOR gate, and driving capability of M6 should be high enough than M4. Also for inputs '000' and '110', output of first XOR gate is '0' and when Cin=0, this enables transistors M2 and M3 simultaneously giving a degraded Sum output. Fig.2 shows the input-output waveform of 8T full adder in Figure 1.

3. PROPOSED 9T FULL ADDER DESIGN

The circuit shown in Figure 3 is the modified 8T full adder cell using an extra transistor M9 is added to improve the performance of the full adder cell. In the circuit of Fig.1 when inputs are ABCin=000, 010 and 110 then problem persists as two transistors get ON simultaneously at the second stage of XOR and results into the degradation of Sum output due to reduced device resistance as the ON transistors will have combined parallel effect on resistance. This problem is eliminated in the circuit of Fig.3 by adding an extra transistor M9. Now with inputs 010 and 100, the first stage XOR gate gives '1' which enables the extra added NMOS M9 giving complete '0' and for Cin=0 disable M4. Thus only M6 get ON produce the Sum output eliminating the problem of simultaneous enabling of two transistors and hence the output degradation will be removed. This reduces the threshold loss problem and also improves the speed of the circuit besides giving full swing output. Figure 4 shows the in-out waveform of proposed circuit.

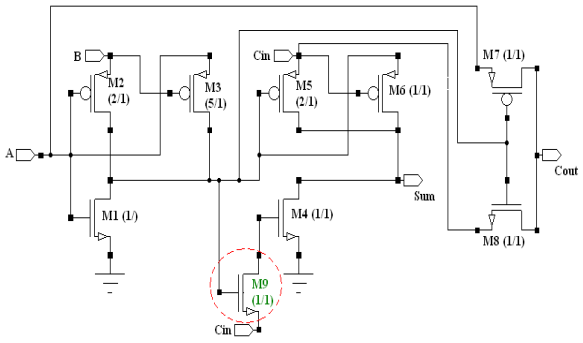

Fig 3: Proposed 1-bit 9T Full Adder

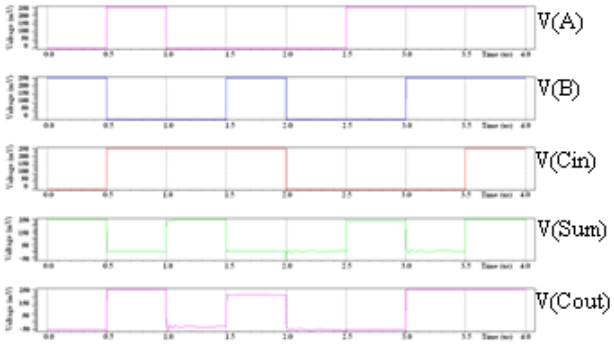

Fig 4: In-out waveform of 1-bit 9T Full Adder

It has area overhead of one transistor but still its power consumption is reduced than the 8T adder circuit. The data given in Table 1 are verified through In-out waveforms of 8T and 9T full adders and proves that proposed circuit has less threshold loss. The 8T full adder in Figure 1 has the 5/1 aspect ratio of transistor M6 in order to drive the Sum output to logic high when inputs are 010 but the adder shown in Figure 2 has 1/1 aspect ratio of transistor M6 to drive the Sum output to logic high and also the extra added transistor M9 has the same aspect ratio. In a nutshell, the proposed 9T full adder has better performance than the earlier designed 8T full adder.

4. SIMULATION & PERFORMANCE

We have performed simulations using Tanner EDA tool at 45nm technology in subthreshold region; with input voltage ranges from 0.1v to 0.25v in the steps of 0.05v. To establish an impartial testing environment both circuits have been tested on the same input patterns which covers all the combination of input stream.

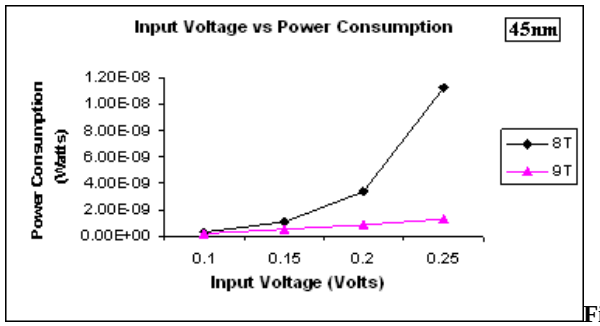

Fig 5: Input Voltage vs Power consumption

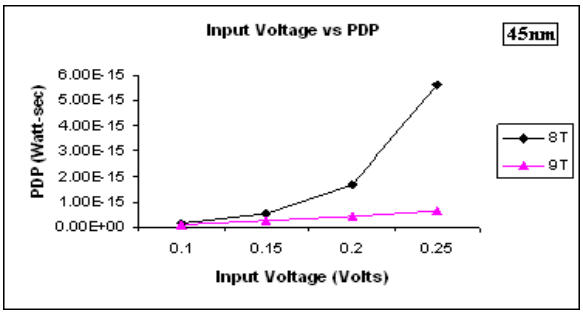

Fig6: Input Voltage vs Power-delay product

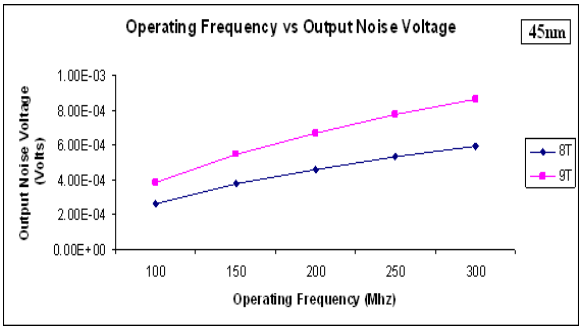

Fig 7: Operating frequency vs Output Noise voltage

Figure 5-7 reveals that the proposed 9T full adder cell proves its superiority in terms of power, power-delay product and noise immunity over existing 8T adder.

5. CONCLUSION

This paper proposes a new improved design of 1-bit full adder cell performing efficiently in subthreshold region outperforming the existing 8T full adder. The combination of improved power dissipation, power-delay product, threshold loss and noise immunity makes the proposed full adder a viable option for ultra low power applications.

6. REFERENCE

[1] Taur, Y, and Ning, T. H. 1998. Fundamentals of modern VLSI devices. Cambridge university press, New York.

[2] Chandrakasan, A. P et.al. April 1992. Low power CMOS digital design. in IEEE Jl. Of solid state circuits, vol. 27, pp. 473-484.

[3] Kim, C. H. and Roy, K. 2002. Dynamic VTH scaling schema for active leakage power reducing in Proceedings of Design Automation and Test in European Conference and Exhibition, pp.163 – 167.

[4] Chowdhury, S. R. Banerjee, A. Roy, A. Saha, H. 2008. A high speed 8 transistor full adder design using novel 3 transistor XOR gates in *International Journal of Electronics, Circuits and Systems* 2, 217

[5] Sharma, T. Sharma, K. G. Singh, B. P. 2010. Energy Efficient 1-bit Full Adder Cell with 45% Reduced Threshold Loss in *International Journal of Recent Trends in Engineering*, Vol 3, pp. 106-110.

[6] Sharma, T. Sharma, K. G. Singh, B. P. 2010. High Performance Full Adder Cell: A Comparative Analysis. *2010 IEEE Student's Technology Symposium* IIT Kharagpur.

[7] Wang, A. Calhoun, B. H. and Chandrakasan, A. 2005. Sub-threshold design for ultra low-power systems. Springer publishers.