Design and Performance Comparison of SOI and Conventional MOSFET based CMOS Inverter

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ABSTRACT
With the emergence of mobile computing and communication, low power device design and implementation have got a significant role to play in VLSI circuit design. Continuous device performance improvement has been made possible only through a combination of device scaling, new device structures and material property improvement to its fundamental limits. Conventional silicon technology has suffered from the fundamental physical limitations in the sub-micron or nanometer region which leads to alternative device technology like Silicon-on-Insulator (SOI) technology. Short-channel-effects (SCEs) reduction, transistor scalability and circuit performance are improved by using Silicon-on-insulator (SOI) technology, especially ultrathin, fully depleted (FD) SOI MOSFETs. SOI-MOSFET provides an advantage for high speed applications because of the low parasitic capacitance. Till now intense interest has been paid in practical fabrication and compact modelling of SOI MOSFET but little attention has been paid to understand the circuit performance improvement with SOI based device compared to bulk MOSFET. In the present analysis CMOS inverters have been designed with latest compact models of SOI and conventional MOSFET using Tanner Simulator. Inverters dc and ac performances have compared to implicate the circuit performance improvement with SOI technology. It has been observed that SOI MOSFET based CMOS inverter shows better dc and ac response in terms of transfer characteristics, gain and frequency response. This is because of less delay factor in SOI MOSFET due to its less parasitic capacitance and better current voltage performance. On the other hand SOI MOSFET based inverter shows higher leakage power because of comparatively lower threshold voltage.

General Terms
SOI MOSFET Performance, SPICE Model of CMOS Inverter, Inverter delay, gain, noise etc.

Keywords
Bulk Silicon MOSFET, SOI MOSFET, BSIM SPICE Model, CMOS Inverter.

1. INTRODUCTION
Presently Complementary MOS (CMOS) technology is widely used to form circuits in numerous and varied applications. Today's computers CPUs and cell phones make use of CMOS due to several key advantages [1]. Till now performance improvement of CMOS technology has been achieved by increasing the speed and decreasing, both the power consumption and size of its two fundamental building blocks, one nmos and one pmos device [2]. As scaling of planar MOS has faced significant challenges, several nonconventional geometry MOS structures have been studied experimentally as well as theoretically in recent time [2].

Among the nonconventional structures, silicon-on-insulator (SOI) technology has received much attention of the researchers due to some of its inherent functional advantages [3]. SOI CMOS technology offers many advantages over bulk silicon (BS) CMOS technology, in particular, higher speed, high radiation tolerance, lower parasitic capacitance, lower short channel effects, better current deliverability, manufacturing compatibility with the existing BS CMOS technology [4].

Intense research on practical fabrication and compact modelling of SOI MOSFET has been carried out during last few decades but little attention has been paid to understand its circuit performance improvement compared to conventional MOSFET [5]. But to understand the true potential of SOI MOSFET as next generation VLSI circuit component, SOI MOSFET based circuit performance analysis is essential. Therefore, in the present analysis two CMOS inverters have been designed, one is with latest compact SOI MOSFETs model and other with latest compact bulk silicon MOSFETs model. Tanner Simulator has been used to compare the ac and dc performance of those inverters.

2. Simulation Model
A CMOS Inverter circuit is composed of two MOSFETs, one pmos (top one) and one nmos (bottom one), as shown in Fig. 1. The body effect is not present in either device since the body of each device is directly connected to the device's source and both gates are connected to the input line. The output line connects to the drains of both FETs.

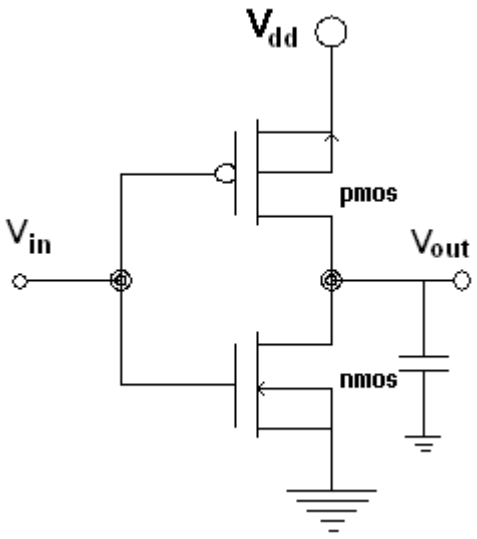

Fig. 1. A Schematic of CMOS inverter

BSIM3 is a physics-based, accurate, scalable, robust and predictive MOSFET SPICE model for circuit simulation and CMOS technology development [6]. Presently, the third iteration of BSIM3, BSIM3v3, has been widely used by most semiconductor and IC design companies world-wide for device modelling and CMOS IC design. In the present case for BS Invertors, BSIM3v3 model has been used which has developed by the BSIM Research Group, University of California, Berkeley [7]. For parasitic specification we have used nmos and pmos model card for BSIM3v3. On the other hand BSIMSOI is a SPICE compact model for SOI circuit design from the same device research group [7]. This model is formulated on top of the BSIM3 framework. It shares the same basic equations with the bulk model so that the physical nature and smoothness of BSIM3v3 are retained. In the present case, very recently developed BSIMSOIv4.4 model has been used for SOI Inverter simulation. Presently this SOI SPICE Model (BSIMSOIv4.4) is not available with Tanner model library but this difficulty has been removed with the inclusion of available verilog-a model along with nmos and pmos model cards [7] in the Tanner model library.

3. SIMULATED RESULTS

Total simulation has been carried out for channel length 250nm and width 2.5 micron and other parameters are set at default model values. The simulated results at nodes ‘in’ and ‘out’ for (Bulk Silicon) BS Inverter and SOI Inverter are reported in the Fig. 2 and Fig. 3 respectively.

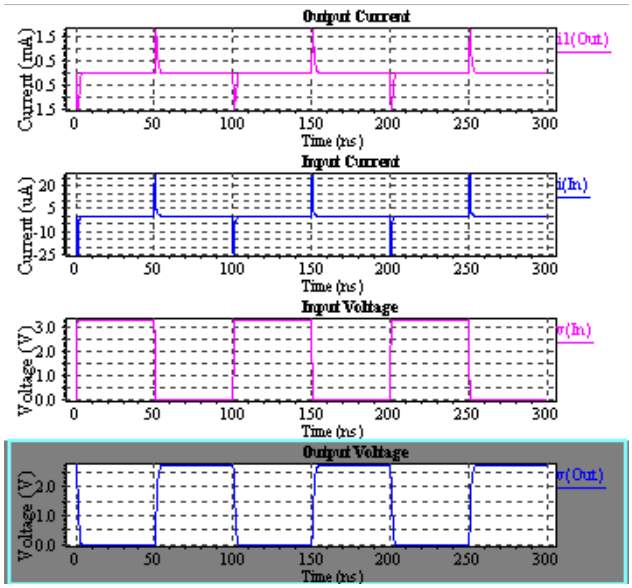

Fig. 2. dc transfer characteristics of BS Inverter

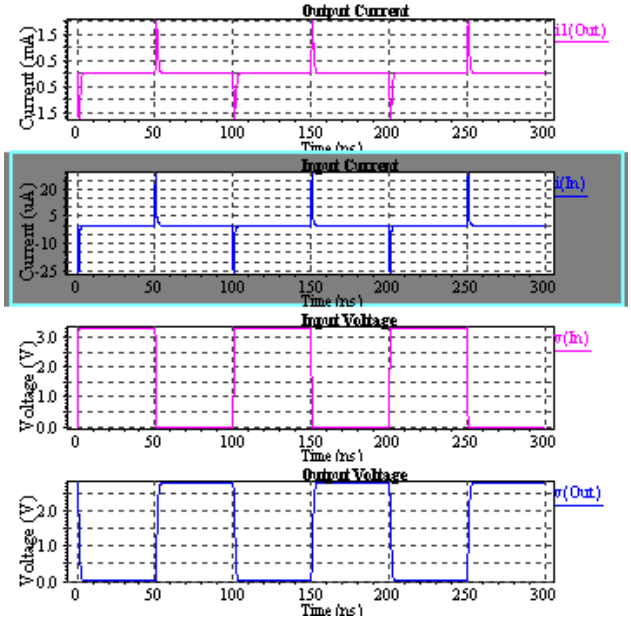

Fig. 3. dc transfer characteristics of SOI Inverter

Table. 1: dc Simulation measurement of BS and SOI Inverter.

Simulation Summary	BS Inverter	SOI Inverter
Rise Delay	$6.6902e^{-10}$ s	$6.6499e^{-10}$
Fall Delay	$1.0931e^{-9}$ s	$0.88209e^{-9}$
Avg. Delay	$8.8105e^{-10}$ s	$7.7354e^{-10}$
Peak Leakage Power	3 mW	5.1 mW

It is clear from the Fig. 2 and Fig.3 that SOI Inverter has faster switching speed as delay is less due to its less RC time constant which is initiated with less parasitic capacitance in SOI MOSFET. On the other hand BS Inverter has less 'peak leakage power' since BS MOSFET has comparatively higher threshold voltage then the SOI MOSFET.

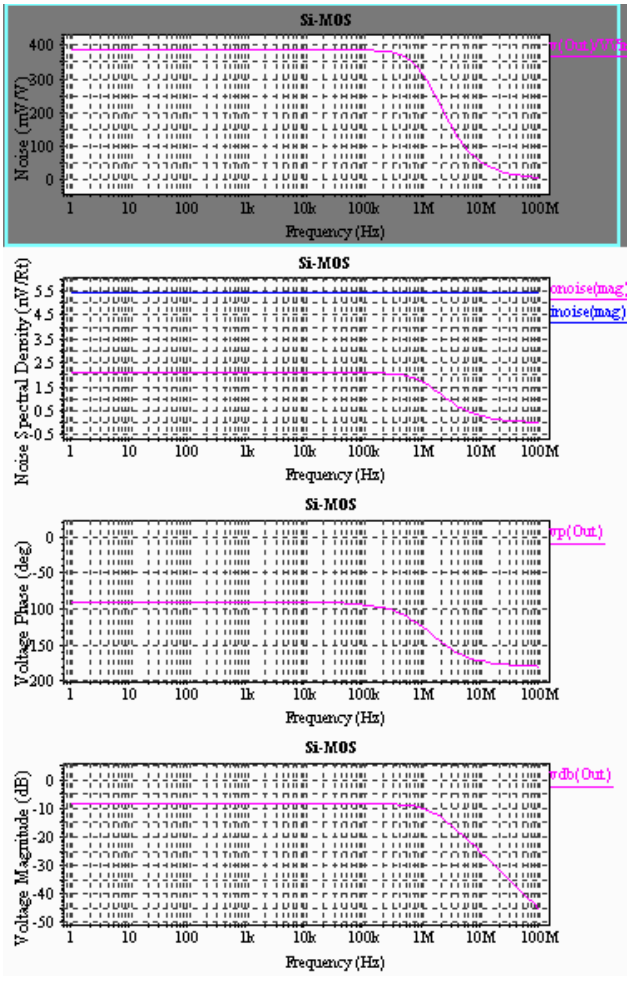

Fig. 4. ac performance of BS Inverter

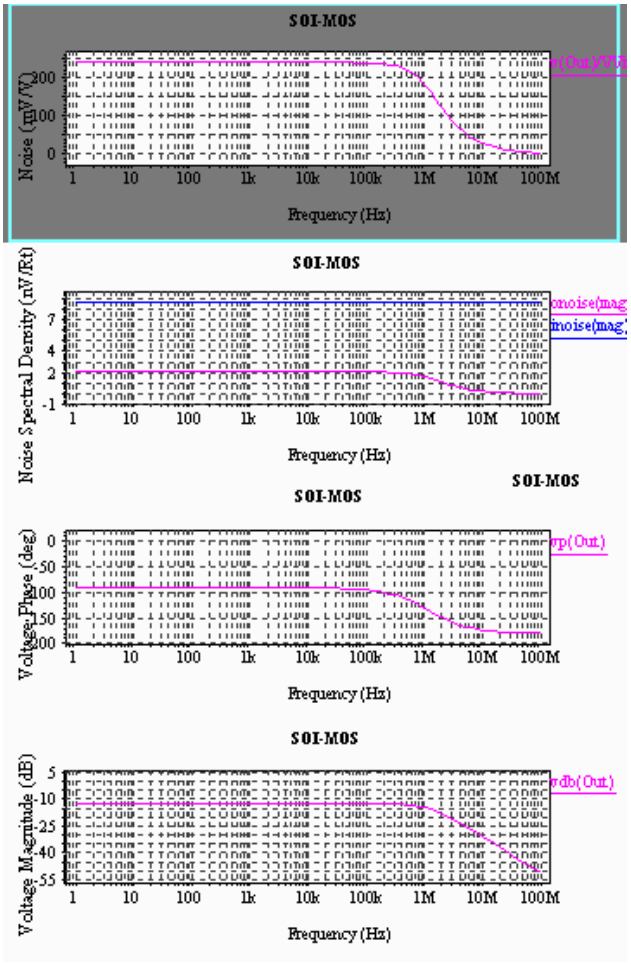

Fig. 5. ac performance of SOI Inverter

The ac behavior of inverter circuit's dependents on dc biasing voltage, small-signal input frequency. For present ac simulation V_{dd}=5V, V_{in}=2V, ac signal magnitude=1V, ac phase=1 to 90 degree, frequency range= 1 Hz to 100 MHz and simulated results are plotted in Fig. 4. and Fig.5 for BS Inverter and SOI Inverter respectively.

Table. 2: ac Simulation measurement of BS and SOI Inverter.

Simulation Summary	BS Inverter	SOI Inverter
Maximum Gain	-8.2484 db	-11.3474 db
Band Width	1.2 MHz	1.4 MHz
Gain band Width Product	9.88MHz	15.88MHz

It is clear from the Fig. 4 and Fig. 5 that noise factor is lower for SOI Inverter because of better channel isolation of SOI MOSFET compared to BS MOSFET. Better current deliverability initiates higher conductance which results higher gain in SOI MOSFET as well as in SOI Inverter. Frequency response is also better due to parasitic capacitance reduction in SOI MOSFET so overall gain-bandwidth product is sufficiently high for SOI Inverter compared to BS Inverter.

4. CONCLUSION

It has been observed that SOI MOSFET based CMOS inverter shows faster switching action compared to conventional MOS based inverter due to less delay. Through ac analysis it has been revealed that noise margin, gain, frequency band width, gain-bandwidth product all are improved when bulk silicon nmos and pmos are replaced with SOI MOSFETs in an Inverter circuit. This circuit performance improvement has been achieved with the inherent functional advantages of SOI MOSFET compared to its bulk silicon counterpart. Only disadvantage found with SOI inverter is higher power consumption due to higher leakage power and that is because of lower threshold voltage of SOI MOSFET. Similar type analysis can be carried out for other circuits also to validate the candidature of SOI technology as a suitable nanoscale CMOS technology.

5. ACKNOWLEDGMENTS

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