Abstract

The drain current model of symmetrical Underlap DGMOSFET is evaluated for subthreshold region. Model data is verified with simulation data for validation of the proposed model. For validation the drain current is evaluated with respect to gate to source potential. The drain current is calculated with variation of gate length, underlap length and silicon body thickness. As the gate length and underlap length increases, the drain current decreases and as silicon body thickness increases, increase of drain current is observed.

References


Index Terms

Computer Science
Integrated Circuit
Keywords
Drain Current  Ultrathin Body  Virtual Source  Underlap Dgmosfet