Abstract

In this paper, we present a performance comparison of existing clocked dynamic comparators. As delay is directly correlated with the submicron scaling, we investigate the performance of the above comparators in terms of delay and Power-Delay Product (PDP). PDP gives the average energy dissipated by the comparator for a single comparison. Simulation results using Mentor Graphics revealed better performance of High Speed Dynamic Comparator (HSDC) compared
Performance Analysis of High Speed Double Tail Dynamic Comparator

Implementation results reveal that high speed dynamic comparator has energy dissipation of 25.14% less compared to the best of the designs used for comparison when operated at 50 MHz.

References

- S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for

**Index Terms**

Computer Science

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**Keywords**

Clocked Dynamic Comparator, Analog-to-digital Converters (adc), Common Mode Voltage