Image compression is the science of reducing the size of image file in bytes by reducing the redundancy between pixels in an image without degrading the quality of image so that it can store more images in a given amount of disk or memory space and also it tends to reduces the time required to send the images over the network. Many hardware efficient techniques exist, inspired from it this paper, propose an image compression technique based on the pixel-wise fidelity and its FPGA implementation. The proposed method is used to reduce the bit
rate of the pixels for better image compression by using angular transformation. Here propose an hardware efficient FPGA architecture using angular domain concept based on CORDIC algorithm is presented. In this paper, the architecture is first simulated in MATLAB for calculating PSNR, MMSE and compression ratio and then it simulated and synthesized using Xilinx ISE tool and verify the parameters such as area, power and delay required for compressing the image with visual appearance of the output compressed image.

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