Abstract

Low-power design is becoming a crucial design objective for the chip design engineer due to the growing demand on portable application and the increasing difficulties in cooling and heat removal. In the integrated circuits power consumption is one of the challenges like area and speed. In this paper a novel technique is proposed to design an error detector for the lower power consumption. Here the work has done by using two low power flip flops (1)have
Low Power error Detector Design by using Low Power Flip Flops Logic

considered SVL5T TSPC FF method and (2) low power DFF. In the proposed system reduction of power is about 50% - 70%. Some of the low power flip flop is also used in multimedia and phase detector application.

References

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Trends in information, Telecommunication and Computing.

Index Terms

Computer Science          Applied Electronics

Keywords
Flip Flop   Low Power Logic   Tspc   Double Edge Triggering   Svl   Error Detector.