Abstract

With the emergence of mobile computing and communication, low power device design and implementation have got a significant role to play in VLSI circuit design. Continuous device performance improvement has been made possible only through a combination of device scaling, new device structures and material property improvement to its fundamental limits.
Conventional silicon technology has suffered from the fundamental physical limitations in the sub-micron or nanometer region which leads to alternative device technology like Silicon-on-Insulator (SOI) technology. Short-channel-effects (SCEs) reduction, transistor scalability and circuit performance are improved by using Silicon-on-insulator (SOI) technology, especially ultrathin, fully depleted (FD) SOI MOSFETs. SOI-MOSFET provides an advantage for high speed applications because of the low parasitic capacitance. Till now intense interest has been paid in practical fabrication and compact modelling of SOI MOSFET but little attention has been paid to understand the circuit performance improvement with SOI based device compared to bulk MOSFET. In the present analysis CMOS inverters have been designed with latest compact models of SOI and conventional MOSFET using Tanner Simulator. Inverters dc and ac performances have compared to implicate the circuit performance improvement with SOI technology. It has been observed that SOI MOSFET based CMOS inverter shows better dc and ac response in terms of transfer characteristics, gain and frequency response. This is because of less delay factor in SOI MOSFET due to its less parasitic capacitance and better current voltage performance. On the other hand SOI MOSFET based inverter shows higher leakage power because of comparatively lower threshold voltage.

Reference

7. BSIMSOI, available at http://www-device.eecs.berkeley.edu/~bsimsoi/

Index Terms

Computer Science  Communications
Key words

SOI MOSFET  Bulk Silicon MOSFET
BSIM SPICE Model
CMOS Inverter