Implementation of Tunable and Non-Tunable Pseudo-Resistors using 0.18µm Technology

Abstract

in integrated circuits implemented to attain high value resistance. Incremental resistance for both non-tunable, tunable pseudo-resistor has been estimated in Cadence Analog Design Environment using 0.18µm technology. Pseudo-resistors make use of diode-connected MOS devices working in subthreshold region and consume less area as compared to the discrete counterpart. Different V-R curves for both non-tunable and tunable pseudo-resistors are obtained and a comparison is presented in terms of linearity and consistency. Low tuning voltages, currents and smaller W/L ratios are selected for analysis to obtain high value resistors greater than 10^{11} Ω. It also leads to the design of Low power integrated circuits.
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References


Index Terms

Computer Science
Circuits And Systems
Keywords
Tunable Pseudo-resistors  Topologies  Integrated Circuits  Subthreshold Region.