Abstract

Computer architecture researchers evaluate key areas such as pipelining, organization, instruction issue, branching, and exception handling when considering asynchronous and synchronous design and implementation trade-offs. Asynchronous or clockless designs are considered as an alternative to conventional synchronous digital system design. The major advantages of asynchronous are low power consumption, better modularity, higher robustness and higher speed. Virtually all processors are synchronous which are based on internal timing devices / circuits that regulate processing. As system becomes increasingly large and complex, this timing device a clock can cause big problems with clock skew and timing delay can create
havoc with the overall design. It can also increase the circuit silicon and power dissipation. To overcome above limitations asynchronous design is considered aggressively. Each subsystems or functional blocks may be optimized without being synchronized to a global clock that may simplify interfacing. Thus the performance of the asynchronous system exhibits the average performance of the overall subsystems or functional block. Furthermore, asynchronous processors may yet prove to offer reduced power dissipation by inherently shutting down unused portions of the circuit.

References

- K. T. Christensen et al., "The Design of an Asynchronous TinyRISC TR4101 Microprocessor Core," in IEEE International Symposium on Advance Research in
Asynchronous Circuit Design for Wireless Sensor Nodes: A Survey

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Index Terms

Computer Science
Circuit Design

Keywords