Low Power Consumption Low Noise Amplifier for 1-10GHz Application

Veena Upadhyay
Electronics & communication engineering
NIIST, Bhopal India

Puran Gour
Electronics & communication engineering
NIIST, Bhopal India

Braj Bihari Soni
Electronics & communication engineering
NIIST, Bhopal India

ABSTRACT
In this paper low power consumption amplifier is presented. Low power consumption amplifier is versatile demanded in modern technology, modern technology want such type of amplifier which gives low power consumption with less reflection, in this paper presented series and shunt feedback topology with pole zero compensation method for designing of low power consumption amplifier, Today the demand of integrated circuits are increasing day by day with increase in the number of elements in it. However, power and reflection should be less. The scaling of the components increase, increase its number, for the similar area of an chip reduces its sub-threshold voltage with its increase in the leakage power consumption.. The Power consumption is based on the number of elements and routing of components and its process fabrication. In this paper developed method to reduce leakage power consumption with reduction of reflection. Here design low power dissipation amplifier using compensation and feedback technique

Keywords
Leakage power dissipation; feedback topology; Transistor;-pole-zero Compensation technique

1. INTRODUCTION
The enhancement in the functioning and performance of an integrated circuit with high density leads to scaling of its featured size and threshold voltage. To maintain the characteristics of MOSFET the power supply voltage is also being reduced. This scaling leads decrement in threshold voltage of the circuit and exponential rise in its leakage power consumption [3]. Technology scaling reduces the gate oxide thickness and the gate length thereby increasing the transistor density and also reduces the delay. Reduced gate lengths result in an increase in the leakage power dissipation. Increased transistor densities result in an increase in the power dissipation per unit area thereby creating hotspots. Scaling down the supply voltage reduces the switching power dissipation. Threshold voltage is simultaneously scaled down along with the supply voltage significantly increasing the leakage power dissipation. LOW-POWER monolithic amplifiers are a critical building block in short-range wireless sensor systems for patient monitoring, implante d biomedical, and radio frequency identi-fication applications. For wireless sensor networks, ultra-low dc-power consumption is a key design issue because of the limited capacity of the small-size battery power source [10]–[13]. By utilizing a variety of low-power design techniques, low dc-power consumption in the deep milli-watt (mW) range has been attain ed in conventional transistor-based amplifiers [10]–[13]. In order to reduce the power dissipation significantly to sub-mW levels, a reflection-type amplifying topology using negative differential resistance (NDR) devices such as tunneldiodes, HITDs (heterojunction interband tunneling diodes), and RTDs (resonant tunneling diodes) can be employed [4]–[6].This topology's unique power-efficient amplification principlewith a gain characteristic, which is achieved almost indepen-dently of the bias current, enables utilization of NDR-based microwave amplifiers in ultra-low-power applications [5]. In a previous work, presented preliminary experimental results of an RTD-based reflection-type microwave amplifier, showing low-power consumption of 470 at 5 GHz [6].

2. PROPOSED BROAD-BAND LNA DESIGN
The objective of the proposed work is to design an amplifier with broad impedance matching with less power consumption. Fig. 1 shows the schematic of the proposed broadband LNA. This amplifier design for 1GHz to 10GHz application. First stage consist of series inductance to provide high input impedance. In second stage used double pole compensation technique to improve impedance bandwidth of amplifier, the value of all elements find out by resonance theory, to reduce the noise figure induced feedback inductor, high mobility NMOS transistor used for design amplifier. The optimal value of 1.8 V for better linearity, the optimization of the proposed work is carried out with the consideration of gain, bandwidth and noise figure. The It should be noticed that there is an equivalent inductance generate due series inductance and feedback mechanism and internal capacitive of MOSFET in the model which makes wideband input matching possible. Overall improves input impedance matching and reduce reflection of proposed design, the second and buffer circuit are used to further extend the bandwidth using inductive-series and feedback technique. The buffer circuit is the cascode configuration which gives sufficient input-output isolation and provides signal amplification. In lat stage inductor and resistor used in series in load at the buffer stage to eliminate the output parasitic capacitance and exist broad band output matching. The series inductor is sized to 100fH so that its parasitic capacitance due to the output stage would not cause reflection degradation at tens of GHz range. As shown in Fig. 2,the simulated power dissipation is between 1-10 GHz which exhibits over 10GHz bandwidth improvement compared with the conventional topology. The simulated noise figure gives minimum value at relatively high frequency between 1-10GHz.

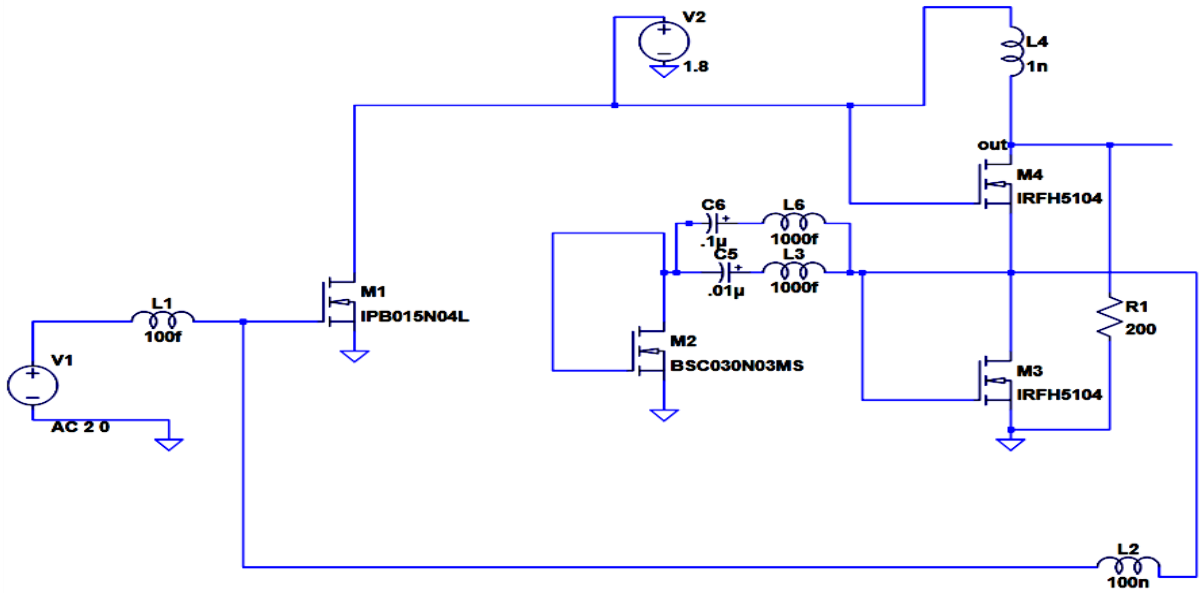

Figure 1 Proposed Amplifier design

3. MEASUREMENT RESULTS

The proposed design is design and validated in LT-Spice simulator. Fig. 2 shows the S-Parameters Shows reflection of proposed design. The proposed LNA achieves a S11≤ -13.9dB, between 1-10GHz.

3.1 S11 Reflection analysis

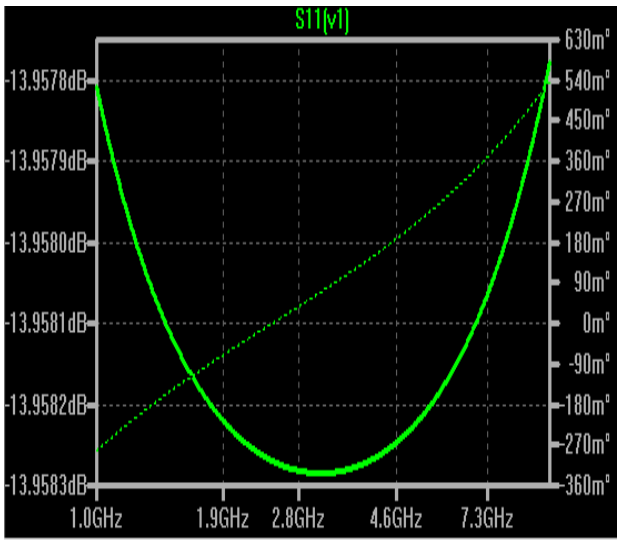

Figure 2 Measured S-parameters

The measured noise figure varies from 0.4 to 0.8 dB with minimum at about 10 GHz as shown in Fig. 4, However, it degrades in low frequencies due to the gain decrease caused by the internal capacitor of MOSFET. Table I compares the proposed work with other reported state-of-art Broadband LNAs design using nano-scale CMOS technology process [4]–[8]. where are the minimum noise figure and minimum power dissipation over the broad bandwidth from 1-10GHz, The proposed work shows excellent performance in terms of its large bandwidth, acceptable I/O return losses verified by S11 Parameters and very less power consumption.

3.2 Power Dissipation Analysis

Figure 3 Power Dissipation analyses

Power dissipation shown in figure 3 this low noise amplifier exist power consumption up to 648uW, power consumption of proposed amplifier is control by using appropriate gate charge and on resistance of transistor, power consumption also control by using reflection elimination method.

3.3 NOISE ANALYSIS

Noise analysis is a important and demanded in designing of recent amplifier in section 3.3.1 input noise analysis is given and in 3.3.2 out noise analysis is given.

3.3.1 Input noise analysis

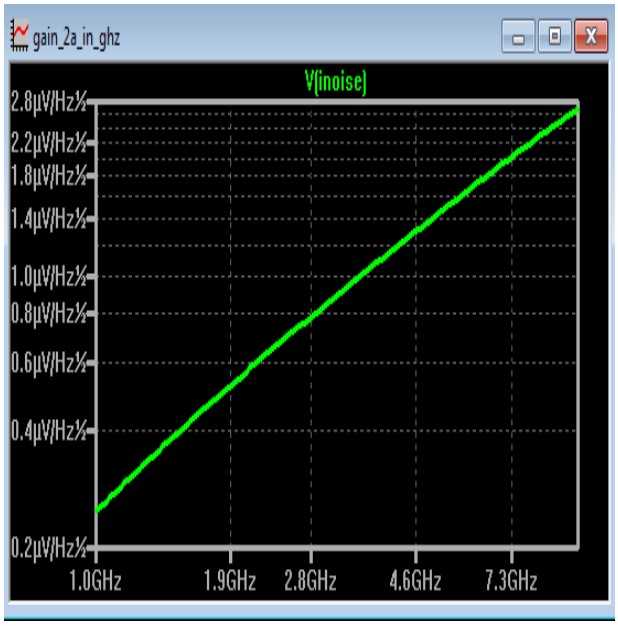

Fig 4 Input noise analysis

Input noise input in amplifier using source is up to 2.8Uv/√Hz. Input noise with respect to frequency is shown in fig 4

3.3.2. Output noise analysis

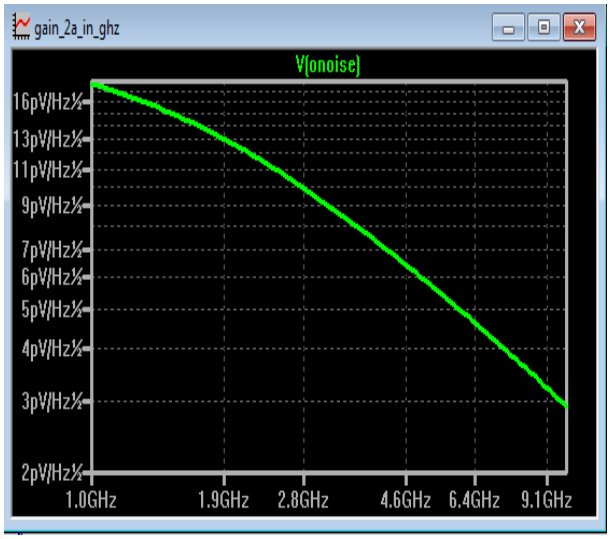

Figure 5 Output noise analysis

Out noise analysis is shown in fig 5, from this fig concluded that noise in output of amplifier obtain from 3pV/√Hz to16pV/√Hz, this ratio shows noise rejection capability of amplifier.

$$Noise\ Figure = 10log\ \frac{input\ Noise}{OUT\ noise}$$

Obtain Noise Figure up to .4 to .8dB

Table I Comparison of Proposed Work with Literatures

Ref	Freq (GHz)	NFmin (dB)	S11 (dB)	Power Dissipation (mW)
[7]	35-44	4.6	≤-7	15
[8]	17.5-26	3.3	≤-6	5.6
[9]	2.1-39	4.5	≤-8	25.5
This Work	1-10	.4 to .8	≤-13.9	648uW

Power dissipation shown in Fig. 3. Achieve Power consumption up 648uW, Validation of work is shown in Table-I, simulation done from 1-10GHz.

4. CONCLUSION

A 1-10 GHz broadband LNA with a power consumption of 648uW. LT-Spice simulator used for designing and validation of proposed amplifier. A series inductor, feedback inductive technique and double pole zero compensation technique is used to achieve excellent input and out matching over a large bandwidth. In ourtput stage buffer and inductive load is used to eliminate reflection and to provide isolation between input and output stage, this stage also exist low power consumption. a minimum 0.4 to 0.8 dB NF and a S11≤-13.9dB, are achieved from 1GHz to 10GHz. The proposed amplifier presents a broad bandwidth

5. REFERENCES

[1] C. Pavageau, M. S. Moussa, J.-P. Raskin, D. Vanhoenaker-Janvier, N. Fel, J. Russat, L. Picheta, and F. Danneville, "A 7 dB 43 GHz CMOS distributed amplifier on high-resistivity SOI substrates," IEEE Trans. Microw. Theory Tech., vol. 56, no. 3, pp. 587–598, Mar. 2008.

[2] S. Chen, J. Kuo, C. Lin, M. Tai, and H. Wang, "A DC-11.5 GHz low-power, wideband amplifier using splitting-load inductive peaking technique," IEEE Microw. Wireless Compon. Lett., vol. 18, no. 7, pp. 482–484, Jul. 2008.

[3] P. Chang and S. Hsu, "A compact 0.1–14 GHz ultra-wideband lownoise amplifier in 0.13 m CMOS," IEEE Trans. Microw. Theory Tech., vol. 58, no. 10, pp. 2575–2581, Oct. 2010.

[4] M. Chen and J. Lin, "A 0.1–20 GHz low-power self-biased resistivefeedback LNA in 90 nm digital CMOS," IEEE Microw. Wireless Compon. Lett., vol. 19, no. 5, pp. 323–325, May 2009.

[5] M. Okushima, J. Borremans, D. Linten, and G. Goeseneken, "A DC-to 22 GHz 8.4 mW compact dual-feedback wideband LNA in 90 nm digital CMOS," in Proc. IEEE RFIC Symp., Jun. 2009, pp. 295–298.

[6] H.-K. Chen, Y.-S. Lin, and S.-S. Liu, "Analysis and design of a 1.6–28 GHz compact wideband LNA in 90 nm CMOS using a -match input network," IEEE Trans. Microw. Theory Tech., vol. 58, no. 8, pp. 2092–2014, Aug. 2010.

[7] H.-C. Yeh, Z.-Y. Liao, and H. Wang, "Analysis and design of millimeter-wave low-power CMOS LNA with transformer-multicascode topology," IEEE Trans. Microw. Theory Tech., vol. 58, no. 8, pp. 3441–3454, Dec. 2011.-

[8] M.-H. Tasi, S. S. H. Hsu, F.-L. Hsueh, C.-P. Jou, and T.-J. Yeh, "A 17.5–26 GHz low-noise amplifier with over 8 kV ESD protection in 65 nm CMOS," IEEE Microw. Wireless Compon. Lett., vol. 18, no. 7, pp. 483–485, Sep. 2012.

[9] Chen Feng, Xiao Peng Yu, et.al. "A Compact 2.1–39 GHz Self-Biased Low-Noise Amplifier in 65 nm CMOS Technology" IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 23, NO. 12, DECEMBER 2013 pp 1531-1309

[10] D. Wu, R. Huang, W. Wong, and Y. Wang, "A 0.4-V low noise ampli-fier using forward body bias technology for 5 GHz application,"IEEE Microw. Wireless Compon. Lett., vol. 17, no. 7, pp. 543–545, Jul. 2007.

[11] D. Linten, L. Aspernyr, W. Jearnsaksiri, J. Rarnos, A. Mercha, S. Jenei,S. Thijs, R. Garcia, H. Jacobsson, P. Wambacq, S. Donnay, and S. De-coutere, "Low-power 5 GHz LNA and VCO in 90 nm RF CMOS," in IEEE Symp. VLSI Circuits Tech. Dig., 2004, pp. 372–375.

[12] .Chang,J.Chen,andY.Wang,"Afully-integrated5GHz low-voltage LNA using forward body bias technology,"IEEE Microw. Wireless Compon. Lett. , vol. 19, no. 3, pp. 176–178, Jul. 2009.

[13] M. Hines, "High-freque ncy negative-resistance circuit principles for esaki diode applications,"Bell Syst. Tech. vol. 39, pp. 477–514, May 1960.