Universal Filter Design using 45nm CMOS-based DDCC for Bluetooth/ Zigbee Applications

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ABSTRACT
The limited performance of voltage mode Op-amps such as bandwidth, slew-rate etc. led the analog designer to search for other possibilities and other building blocks. Thus the current-mode active building blocks received considerable attention due to their larger dynamic range, high frequency, lower power consumption, high slew rate, better linearity, better accuracy and higher bandwidth. In this paper, a universal filter has been designed using Differential Difference Current Conveyor (DDCC) as an active building block. The filter provide low pass, high pass and band pass responses. The filter is also tuned for Zigbee and Bluetooth standards. The filter offers high bandwidth. The circuit implemented using DDCC provide non-interactive frequency control and employ only the grounded capacitors. The performance of the circuit is confirmed from HSPICE simulation results.

General Terms
Current mode circuits, Universal filter, Analog circuit design.

Keywords
Current Mode, Differential Difference Current Conveyor(DDCC), HSPICE, Zigbee, Bluetooth.

1. INTRODUCTION
Over the last few decades, electronic devices have been prominently used in various human's activities. Nowadays electronic devices are used in various applications like communications, defense systems, automation of manufacturing process, entertainment systems, home appliances, computing and are making our life more comfortable and safer [1]-[4]. Although large electronic systems can be constructed almost entirely with digital techniques, many systems still have analog components. This is because signals emanating from storage media, transmission media, and physical sensors are often fundamentally analog. Moreover, digital systems may have to give analog signals as an output to actuators, displays, and transmission media. Therefore, the need for analog interface circuits like filters, analog-to-digital converters (ADC's), phase-locked loops, sample and hold circuits is inherent in such systems [5]. The basic analog electronic circuits include the operational amplifier, inverting amplifier, non-inverting amplifier, integrator, bistable multi-vibrator, peak detector, comparator, filters, RC oscillator, etc. whereas the basic digital building blocks are phase locked loop (PLL), sample and hold etc.

With the advent of integrated circuit technology, it has become possible to design larger electronic circuits on a single chip. Mixed-signal ICs are chips that contain both digital and analog circuits on the same chip. All the above mentioned circuits can be designed individually on a single chip by using either voltage mode or current mode techniques. Similarly, the general trend in CMOS technology is to make the devices smaller and smaller to increase the density and speed of digital circuits [3].

It is also common to reduce the thickness of the gate oxide in order to increase the driving capability of the transistor. In addition, the thickness reduction implies that the supply voltage must be decreased to avoid excessive electric field in the devices. Also the number of components is increasing on a single chip, but it can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating of the chip. Since the introduction of integrated circuits, the operational amplifier (OA) has served as the basic voltage mode building block in analog circuit design. Voltage-mode operational amplifier (OA) circuits have limited bandwidth at high closed-loop gains due to the constant gain-bandwidth product. The moderate slew-rate of the operational amplifier limits the large-signal, high-frequency operation. Also in the applications where wide bandwidth is required, low power consumption and low voltage operation are needed simultaneously. In that case, voltage-mode operational amplifier becomes too complex. Therefore, voltage mode circuits based on operational amplifier (OA) are not suitable for use in high frequency applications. Thus their limited performance as mentioned above, led the analog designer to search for other possibilities and other building blocks. Current mode circuits like current conveyors are getting significant attention in current analog ICs design due to their higher band-width, greater linearity, larger dynamic range, simpler circuitry, lower power consumption and less chip area [6]-[9].

The universal filter is among the most popular analog filters as it can provide several standard functions like low pass, high pass, and band pass. Various simulations have been carried out to verify the linearity between output and input ports, range of operation frequency, etc [10]-[17].

In this paper first DDCC is implemented using different CMOS technologies on HSPICE (i.e. 180nm, 90nm and 45 nm technologies) and simulation results are compared. A universal filter is then designed using 45nm DDCC as a building block and the results are tuned for Zigbee and Bluetooth standards.

2. DIFFERENTIAL DIFFERENCECURRENT CONVEYOR (DDCC)
The differential difference current conveyor (DDCC)has four input signal ports (Y1, Y2, Y3, X)and one output signal port Z. The block diagram of DDCC is shown in Fig. 1.

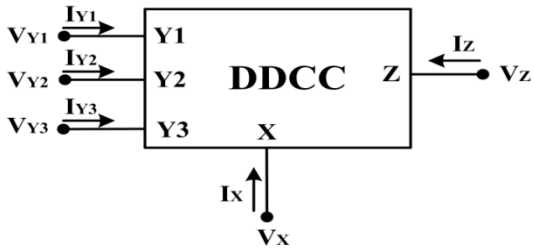

Fig 1: Block Diagram of Differential Difference Current Conveyor (DDCC)

Basically DDCC comprises of second generation current conveyor (CCII) and differential difference amplifier (DDA) and offers advantages such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption and high-input impedance. The input ports Y1, Y2 and Y3 are high impedance ports and the input port X is a low impedance port. Output port Z is high impedance current output port.Fig.2 shows the CMOS-based internal circuit of DDCC. The input-output port relationship is given by the matrix shown in (1.1).

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \quad (1.1)$$

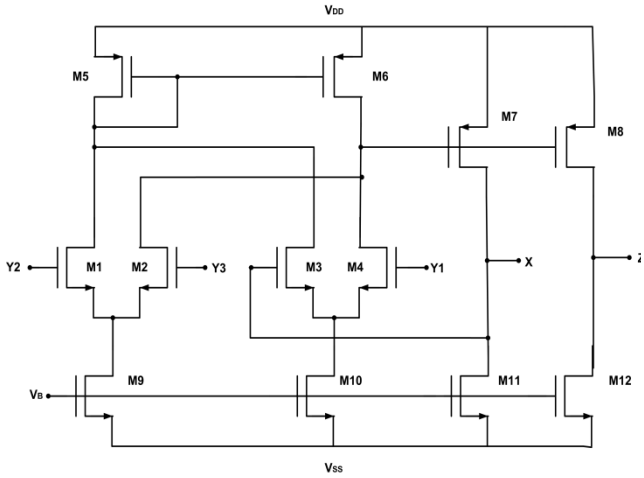

Fig 2. CMOS Implementation of DDCC

The Transient and AC analysis of DDCC were carried out using the computer simulations done in HSPICE. Results of the various device verification tests at 45nm technology are presented in Fig. 3 and Fig. 4. Transient analysis has been carried out with 100MHz sinusoidal input, for which the current relationship equation i.e. $I_Z=I_X$ is successfully verified.AC analysis for the CMOS-based DDCC reveals excellent conformity between the input current (I_X) and the output current (I_Z) till about 10 GHz.

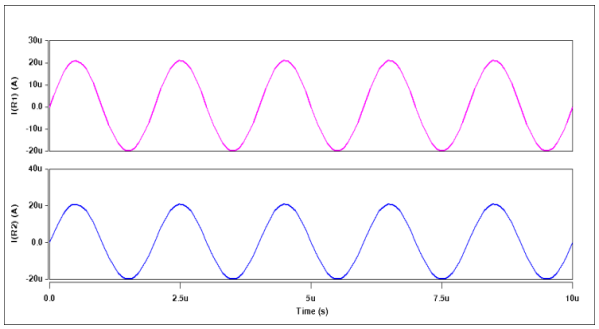

Fig 3. Results of transient analysis using HSPICE simulations for X and Z outputs of DDCC

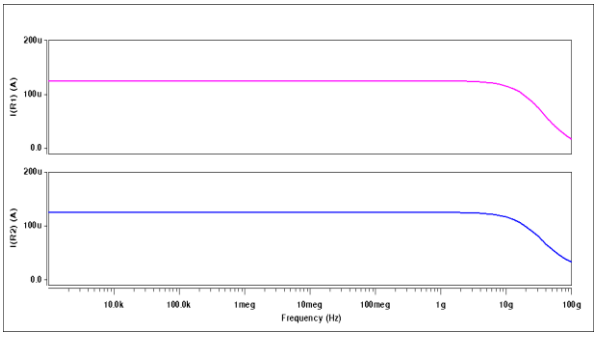

Fig 4.Results of AC analysis using HSPICE simulations for X and Z outputs of DDCC

2.1 Performance Comparison at 180nm, 90nm and 45nm technologies

Performance comparison of the DDCC circut has been done using 180nm, 90nm and 45nm CMOS technology node. Power supplies, bias voltages and the obtained 3-dB bandwidth are shown in Table 1. and simulation results for AC responses are shown in Fig. 5.

Table 1. Performance Comparison at different technologies

Technology	180nm	90nm	45nm
Supply Voltage (V)	1.85	1.5	1.3
Bias Voltage (V)	-1.1	-1	-0.95
3-dB Bandwidth (GHz)	3.03	4.63	23.7

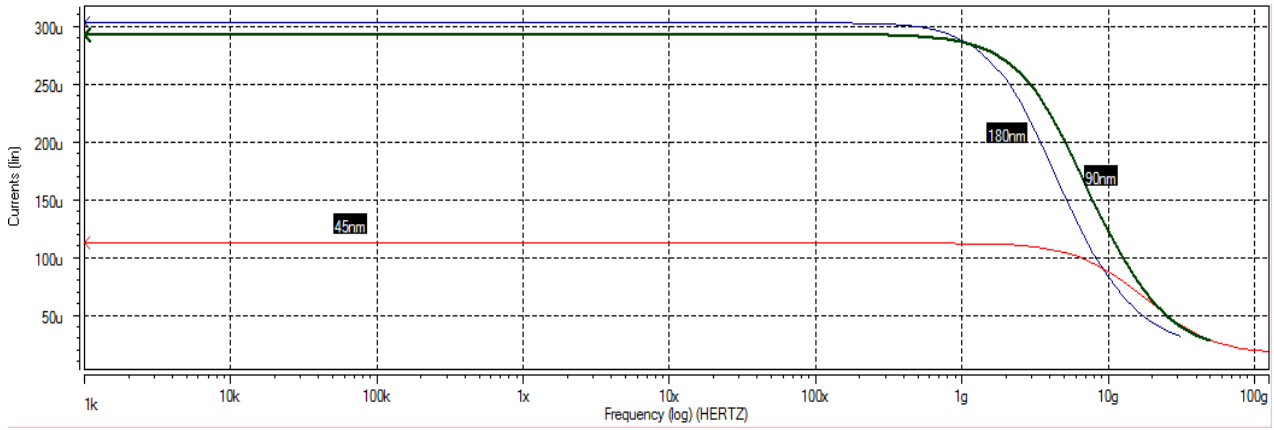

Fig.5.Performance comparison at 180 nm, 90 nm, and 45 nm technologies

3. UNIVERSAL FILTER DESIGN USING DDCC

DDCC are widely used as basic active building blocks to realize various current mode active filters. The universal filter is among the most popular analog filters as it can provide several standard functions like low pass, high pass and band pass. A current mode universal filter has been designed using CMOS-based DDCC of Fig. 2 as an active block. The block diagram of the filter is shown in the Fig.6. The implementation requires only three current Differential Difference Current Conveyor (DDCC) and two grounded capacitors. The filter can provide several functions like low pass, high pass, and band pass.

The relationship between inputs-outputs in Fig. 6 as follows:

Case1: When input is applied at Vin1:
Output is High pass.

Case2: When input is applied at Vin2:
Output is Band pass.

Case3: When input is applied at Vin3:
Output is Low pass.

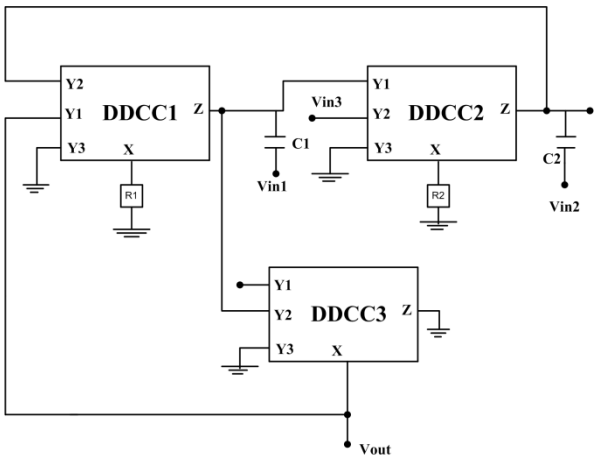

Fig 6. Universal Filter Design using DDCC

The filter operation is verified through HSPICE simulations using the CMOS-based DDCC. Supply voltage used was±1V. The circuit was designed with capacitors of 4fF, and the bias voltages as V_{bb} = 0.9V. The frequency response for low pass, high pass and band pass filter are shown in the Fig. 7-9. The band-width and peak frequency of low-pass, high-pass and band-pass filters are shown in Table 2.The values of capacitors are varied to obtain the full range of Bluetooth and Zigbee standards as shown in Fig. 10 and Fig. 11.

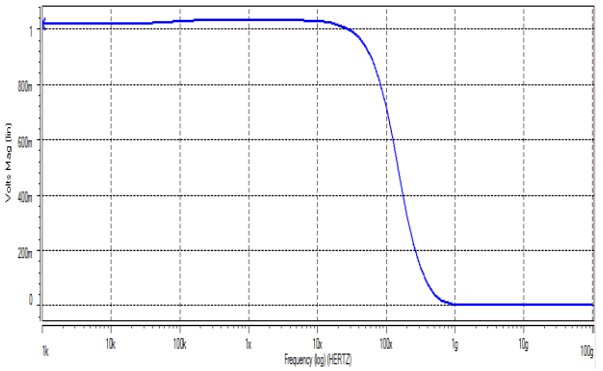

Fig 7 . Low Pass Filter Response

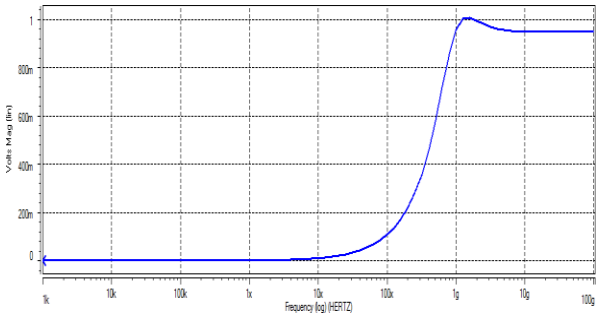

Fig 8. High Pass Filter Response

Table 2. Bandwidth and peak frequencies of various filters

Parameter	Low Pass	High Pass	Band Pass
Bandwidth	622 MHz	218 MHz	2.82 GHz
Peak Frequency	1.46 GHz	40 MHz	3.16 GHz

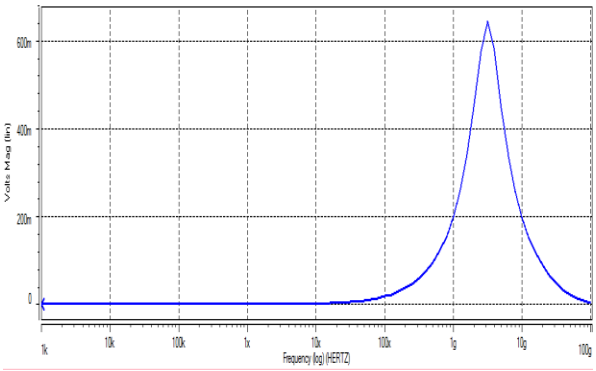

Fig 9 . Band Pass Filter Response

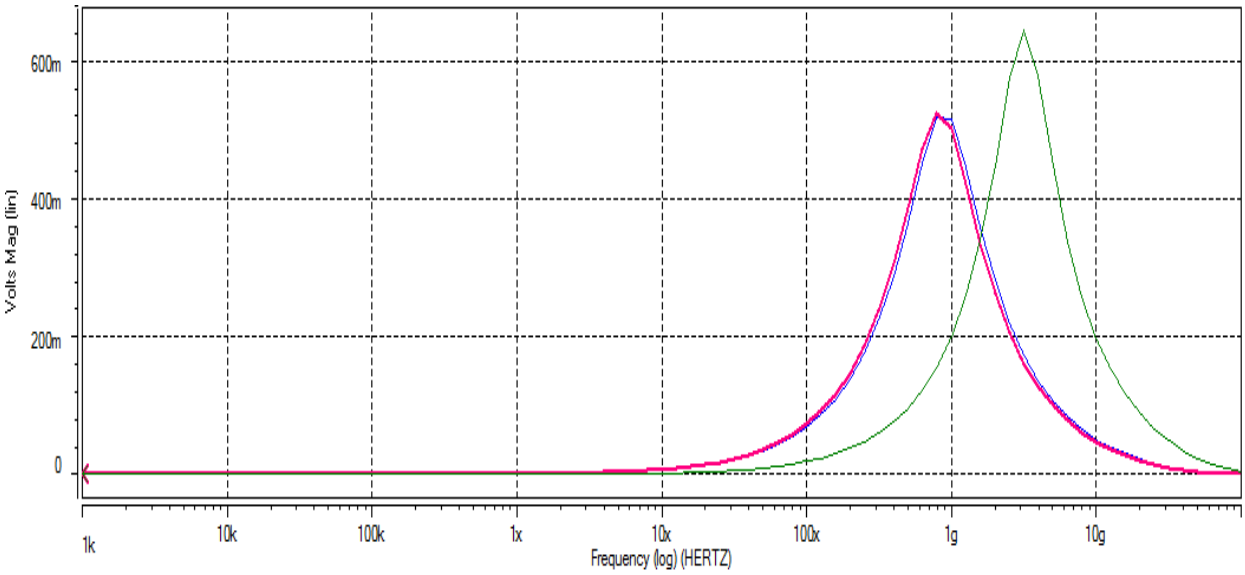

Fig 10. Tuning of Centre Frequency of Band Pass Filter for Zigbee Standard

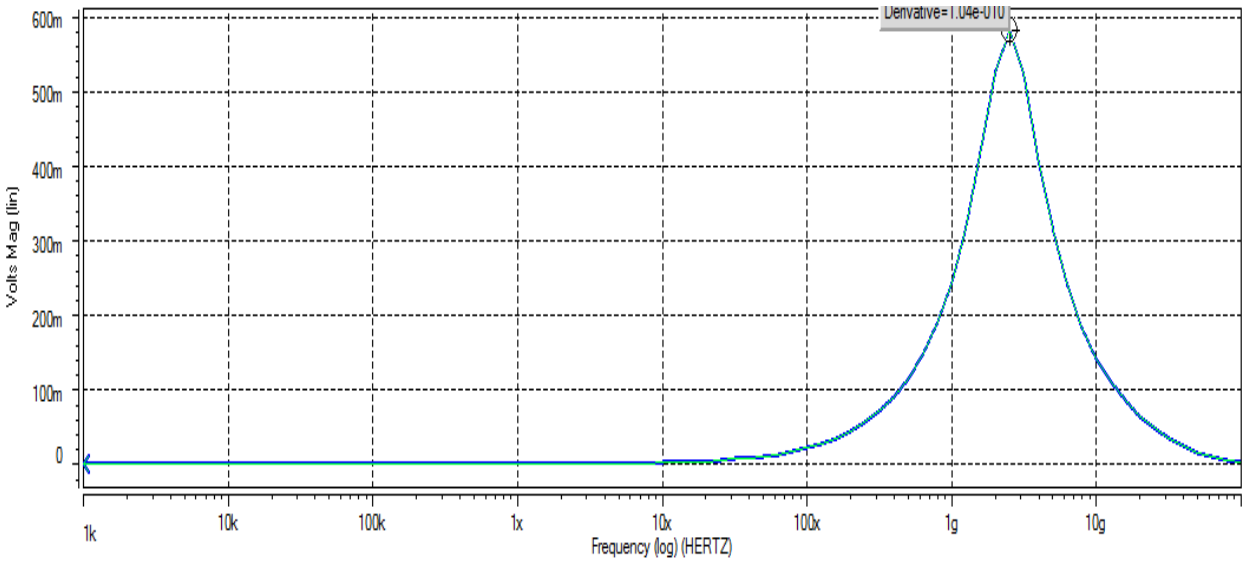

Fig. 11. Tuning of Centre Frequency of Band Pass Filter for Bluetooth Standard

4. CONCLUSION

In this paper, the differential difference current conveyor circuit (DDCC) is implemented using the 45nm CMOS technology. The circuit design is based on a ±1V DC supply and transient and AC analysis are carried out using HSPICE tool. The simulation results indicate the correct operation of the DDCC circuit up to 10 GHz. A current mode universal filter is then discussed that employs CMOS-based DDCC, resistor of low values and grounded capacitors. The filter can be configured to obtain three functions: low-pass, high-pass

and band-pass. The HSPICE simulation results confirmed the suitability of the voltage-mode universal filter for operation in the 868/915 MHz, 2.4 GHz band used by Zigbee standard and 2.4GHz to 2.48 GHz band used by Bluetooth standard. Thus the filter is suitable for the Bluetooth and Zigbee applications. The DDCC can be used as an active building block in the designing of various analog circuits such as oscillators, rectifiers, instrumentation amplifiers etc.

5. REFERENCES

[1] P.E. Allen and D.R. Holberg, "CMOS Analog Circuit Design", New York: Oxford University Press, 2002.

[2] David A. Johns and Ken Martin, "Analog Integrated Circuit Design", WileyIndia Pvt. Ltd., 1997.

[3] K. Bult, "Analog design in deep sub-micron CMOS", Proc. European Solid-State Conf, pages pp. 126-132, 2001.

[4] J. R. Angulo, R.G. Carvajal, and A. L. Martin, "Techniques for the design of low voltage power efficient analog and mixed signal circuits", 22nd International Conference on VLSI Design, Vol. 26, No. 27:pp. 5-9, Jan. 2009.

[5] Lattenberg and Vrba, "Filters with current amplifiers for high-speed communication", International Conference on Systems and Mobile Communications and Learning Technologies, Vol. 150, No. 150:pp. 23-29, Apr. 2006.

[6] H. H. Kuntman and A. Uygur, "New possibilities and trends in circuit design for analog signal processing", International Conference on Applied Electronics, Vol. 1, No. 9:pp. 5-7, Sept. 2012.

[7] K. C. Smith and A. S. Sedra, "The current conveyor- a new building block", Proc. of the IEEE, Vol. 56, No. 8:pp. 1368-1369, Aug. 1968.

[8] I. P. Singh, K. Singh, and S. N. Shukla, "Current conveyor: novel universal active block" Samriddhi-Journal of Physical Sciences, Engineering Technology,Vol. 1, Issue 1, 2010.

[9] F S Gohn A Sedra, G Robert, "The current conveyor: history and progress", IEEE International Symp. on Circuits and Systems, Portland, USA, 3:1567-1570, 1989.

[10] Ahmed M. Soliman El-Adawy, Ahmed A. and Hassan O. Elwan.A, "A novel fully differential current conveyor and applications for analog VLSI", Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions, 4: 306-313, 2000.

[11] H. O. Elwan Alzaher, H. A. and Mohammed Ismail, "CMOS fully differential second-generation current conveyor", Electronics Letters 36.13, pages 1095- 1096, 2000.

[12] H. O. Elwan and A. M. Soliman, "Novel CMOS differential voltage current conveyor and its applications in Circuits, Devices and Systems", IEE Proceedings, 144-3:195-200, 1997.

[13] S-I. Liu H-W. Tsao Chiu, Wenwei and J-J. Chen, "CMOS differential difference current conveyors and their applications", IEE Proceedings-Circuits, Devices and Systems, 143-2:91-96, 1996.

[14] R S Pande R V Yenkar and S S Limaye, "Design and implementation of different generations of current conveyor using 100nm CMOS technology", International Journal of Recent Development in Engineering and Technology(IJRDET Online), 2-3:131-136, 2014.

[15] S. Rana and K. Pal, "Current conveyor simulation circuits using operational amplifiers", Journal of Physical Sciences, Vol. 11:pp. 124-132, Aug. 2007.

[16] J. Sharma, M. S. Ansari, J. Sharma, "Current-mode electronically tunable resistor-less universal filter in 0.5v 32nm CNFET", International Conference on Devices, Circuits and Communications (ICDCCom), 2014 (12-13 Sept. 2014) 1–6.

[17] J. Sharma, M. S. Ansari, J. Sharma, "Electronically tunable resistor-less universal filter in 0.5v 32nm CNFET", Fifth International Symposium on Electronic System Design (ISED) (Dec. 2014) 206–207.