Low Power, Delay Optimized Buffer Design using 70nm CMOS Technology

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ABSTRACT
This paper addresses the issues of power dissipation and propagation delay in CMOS buffers driving large capacitive loads and proposes a CMOS buffer design for improving power dissipation at optimized propagation delay. The reduction in power dissipation is achieved by minimizing short circuit power and subthreshold leakage power which is predominant when supply voltage (V_{DD}) and threshold voltage (V_{th}) are scaled for low voltage applications in deep submicron (DSM) region. The proposed buffer has been designed and simulated using Tanner SPICE tool in 70 nm VLSI technology node. The results show that modified taper buffer design provides 15% reduction in power dissipation at same value of propagation delay when compared with conventional design.

Keywords
CMOS, DSM, Taper Buffer, VLSI

1. INTRODUCTION
Large capacitive loads are often present in CMOS integrated circuits and tapered buffers are used to drive these large capacitive loads at high speed, while ensuring that the load placed on previous stages of the signal path is not too large. These buffers are used in the memory access path as word-line drivers, to drive large off-chip capacitances in I/O circuits, and in clock trees to ensure that skew constraints are satisfied. But, deployment of these buffers in high-performance systems imposes a power overhead on each instance regardless to its actual performance.

High-performance VLSI design is attracting much attention because of emerging need for miniaturization, and hence design optimization for trading-off power and performance in nanometer scale integrated circuits is the need of the present scenario, which demands a decrease in both supply voltage V_{DD} (to maintain low power dissipation) and threshold voltage V_{th} (to sustain propagation delay reduction), but the fact is that the decrease in V_{th} not only increases leakage power but also short circuit power. while working in nano scale technology the total power dissipation of clock drivers, which generally have CMOS inverters, is quite large and have 30 to 50% share only of leakage current and short circuit current [1,2]. To solve this problem of high power dissipation, a design scheme has been proposed, which not only minimizes short circuit power, and leakage power but also optimizes propagation delay [3,4]. So our work presents a CMOS taper buffer design which considers the power dissipation as dominant cost function. The rest of the paper is organized as follows:

In section 2 taper buffer and its design aspects are discussed. Section 3 presents proposed CMOS taper buffer. The concept of power delay optimization is discussed in section 4.The results and discussions are reported in Section 5. Finally, concluding remarks are offered in section 6.

2. CMOS TAPERED BUFFER DESIGN
This section presents the conceptual details of CMOS taper buffer design. In this work, we have extended the split capacitor model of taper buffer given by [5]. The brief of this model is presented in Fig 1.

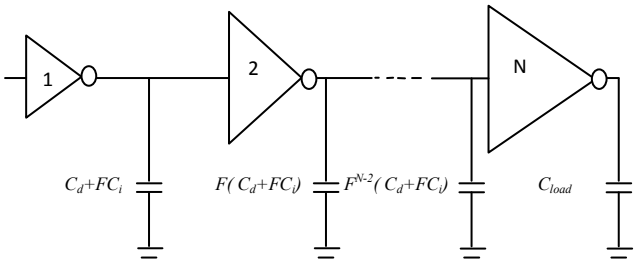

Figure 1: N stage Taper buffer.

The buffer consists of a chain of inverter stages where width of each MOS transistor in a stage is increased by a constant factor (called taper factor) than that of the transistors in the previous stage. The model is named as split capacitor model as output capacitance and input capacitance of each stage is modeled separately. The constant increase in width of transistors in each stage provides fixed ratio of output current drive to output capacitance and hence equal rise, fall, and delay times for each stage. Here C_i denotes the input capacitance of minimum size inverter, C_d denotes the drain capacitance of minimum size inverter, C_{load} denotes the load capacitance of the last stage inverter, N denotes number of stages in the buffer chain and F denotes the scaling factor per stage in the inverter buffer chain.

Design of taper buffer is based on analytical modeling of performance criteria and analyzing them individually with respect to the parameters like capacitive load dependent tapering factor and number of stages, which are the two primary variables in the design of tapered buffers for a specific application [6]. The design we have presented uses two different conditions.

First condition is, when number of buffer stages are $N=N_D$ to achieve minimum propagation delay irrespective of power dissipation.

Second condition is, when number of buffer stages are $N=N_{opt}$ to minimize cost function.

The cost function is based on power (*P*), delay (*D*) product and is calculated depending on the weight of each component in the product which is given by

$$C = P^{a} \times D^{b} \quad (1)$$

If a =1 and b =2 then cost function becomes PD^2 and is suitable for the applications where more weight is required to be given to propagation delay than to power dissipation.

The number of buffer stages required in each of the two design conditions depends on technology dependent tapering factor F, load capacitance and input capacitance of buffer. The F is given by

$$F\left[\ln(F)-1\right]=\frac{C_d}{C_i} \quad (2)$$

Where C_d =drain capacitance, C_i = gate capacitance, C_L = load capacitance.
For the first design condition to achieve minimum delay the number of stages required are given by[6]and are expressed as

$$N_D = \frac{\ln\left(C_L / C_i\right)}{\ln(F)} \quad (3)$$

Similarly for the second design condition to achieve minimum power delay product based on cost function C the number of stages used are

$$N_{opt} = \left[N_D \left(1 - e^{-0.7\left(\frac{b}{a}\right)} \right) - 1 \right] \quad (4)$$

For the design of taper buffer in 70nm technology node the different design parameters are V_{DD} = 1 volt, V_{th} value used is 0.2 volt, C_d =1fF, C_i=1.5fF. Range of capacitive load is C_L =15fF to 150000fF.

In first condition the transistor width of each inverter stage is increased by a factor F_D which depends on number of stages used and ratio of load capacitance to input capacitance[6] and is expressed as

$$F_D = \left(C_L / C_i \right)^{1/N_D} \quad (5)$$

Similarly for the second condition the transistor width factor F_{opt} is given by

$$F_{opt} = \left(C_L / C_i \right)^{1/N_{opt}} \quad (6)$$

The propagation delay in the taper buffer can be calculated using [3,6]and is given by

$$T_{delay} = NV_{DD}\frac{C_d + FC_i}{I_{DO}}\left[\left(\frac{9}{8}+\frac{V_{DO}}{0.8V_{DD}}\ln\left(\frac{10V_{DO}}{eV_{DD}}\right)\right)\left(\frac{1}{2}-\frac{1-v_t}{1+\alpha}\right)+\frac{1}{2}\right] \quad (7)$$

Here I_{D0} is the drain saturation current at $V_{GS}=V_{DD}$,V_{DO} is the drain saturation voltage at $V_{GS}=V_{DD}$, $V_t = V_{th}/V_{DD}$ and α is velocity saturation index.

The power dissipation in the taper buffer has three main components which are dynamic power, short circuit power and subthreshold leakage power hence total power dissipation is given by

$$P_t = P_{dyn} + P_{S.C.} + P_{sub} \quad (8)$$

Analytically the dynamic power and short circuit power dissipation components are described using [3]and[6] and are given as

$$P_{dyn} = V^2_{DD} f (C_d + FC_i)\left(\frac{\frac{C_L}{Ci}-1}{F-1}\right) \quad (9)$$

Where f is the frequency of operation.

$$P_{S.C.} = P_{dyn}\left(\frac{9}{8}+\frac{V_{DO}}{0.8V_{DD}} ln\frac{10V_{DD}}{eV_{DD}}\right)\times\frac{1}{\alpha\text{-}1}\frac{1}{2^{\alpha\text{-}1}}\frac{(1\text{-}2V_T)^{\alpha+1}}{(1-V_T)^{\alpha}} \quad (10)$$

The analytical expression for subthreshold leakage power, which is due to the weak inversion conduction current flowing between the drain and the source when $|V_{GS}| < |V_{th}|$,is stated in [7]and[8] and is expressed as

$$P_{sub} = V_{DD}\, l_{sub}\left(\frac{\frac{C_L}{Ci}-1}{F-1}\right) \quad (11)$$

where

$$l_{sub} = \mu\ C_{dp} v_T^2 \times e^{\frac{C_{ox}(V_{GS}-V_{th})}{C_{dp} v_T}} \times \left(1 - e^{\frac{-V_{Ds}}{v_T}}\right) \quad (12)$$

and C_{dp} denotes the capacitance of the depletion region, V_T is the thermal voltage that is equal to kT/q, C_{ox} is the oxide capacitance per unit area between the gate metal and the bulk surface, V_{GS} is gate to source voltage when MOS transistor is off (0 volt) and μ is the electron mobility.

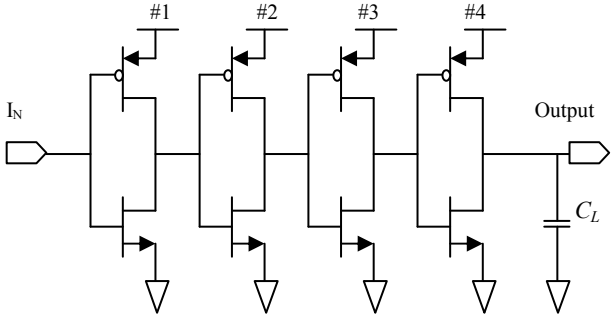

Figure 2: 4 stage Taper Buffer

A 4 stage conventional taper buffer is shown in figure 2 which has capacitive load C_L=150fF and F_D =3.16 when designed for minimum delay condition. The input is applied at I_N and different buffer stages are cascaded to get output across C_L.

3. PROPOSED BUFFER DESIGN

It is well-known that the most of the power dissipation in CMOS structures is caused by charging/discharging the output load and by the short-circuit current that flows from the power supply to the ground, during switching of structures. The importance of short-circuit power dissipation in CMOS buffers, comes from the fact that a great fraction of the energy dissipated in VLSI circuits is due to on-chip and off-chip signal driver circuits, which are based on inverting buffers [9]. In addition, the problem is exacerbated when the input signal operates at high frequencies since the number of times the power dissipates in a specific interval may also be proportionately high [10,11]. So, it is desirable to reduce the short circuit power dissipation. Hence a modified buffer is proposed which dissipates less power because the short circuit component of power is eliminated in the design by tri-stating its output node momentarily before every output signal transition [12] .This is achieved by applying the gate driving signal of PMOS (NMOS) transistor to NMOS (PMOS) transistor of the output stage through a feedback network which delays the driving signal and avoids simultaneous turn on of NMOS and PMOS transistors during signal transition which is the very cause of short circuit current. Further, the capacitive load dependent tapering factor is applied to all the stages including the final stage. Figure 3 shows a 4 stage proposed taper buffer in which input signal is applied at I_N which is amplified by 1st and 2nd stage. The feedback network is applied in 3rd and 4th stage, where T1, T4, T5, T7 are PMOS transistors and T2, T3, T6, T8 are NMOS transistors. INV1 and INV2 are minimum sized inverters which are connected to gate terminals of T8 and T7 for their input and with T2 and T5 as output respectively. The output of 2nd stage is connected toT1, T3, T4 and T6 only.

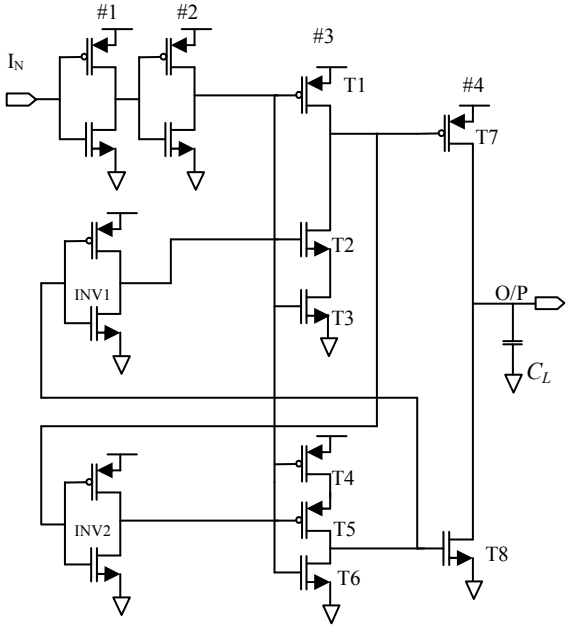

Figure 3: 4 stage modified Taper Buffer

For illustration if we assume that input signal I_N at input terminal is at logic high level causing gate terminals of T7 and T8 to be at a logical low level ("logic low"). The logic low on gate terminal of T7 is fed back through minimum sized inverter INV2 which turns off transistor T5. Thus gate terminal of T8 cannot charge until gate terminal of T7 charges to logic high. Now, assuming that input signal made a transition from a logic high level to a logic low level, transistors T1 and T4 turn on, and transistors T3 and T6 turn off. As a result, gate terminal of T7 charges first to logic high and gate terminal of T8 starts charging after gate terminal of T7 is charged to logic high. Thus, charging of gate terminal of T8 is delayed which may cause a delay in turn on of transistor T8. Similarly, when input signal makes a transition from a logic low to high, gate terminal of T8 discharges first and then gate terminal T7 is discharged. Again, the delay in discharge of gate terminal of T7 may cause delay in turn on of transistor T7. The delay in charging/discharging of gate terminals of T7 and T8 may avoid these transistors being on at the same time and thus reduces the short circuit power dissipation.

4. POWER AND DELAY OPTIMIZATION

Many techniques have been employed to reduce power dissipation in VLSI circuits and lowering the supply voltage V_{DD} is the most effective to decrease the power dissipation, since CMOS power quadrically depends on V_{DD}. However low V_{DD} requires low threshold voltage $V_{th,}$ but then the sub-threshold leakage power increases exponentially. Hence there is a great necessity to optimise V_{th} to achieve the required performance at minimum power dissipation [13,14]. In this context, V_{th} optimization has been investigated extensively with the objective to minimize the power consumption while satisfying a speed constraint.

In our work, power and delay optimisation is achieved by slightly increasing threshold voltage in the proposed design which not only reduces subthreshold leakage power but also optimise delay [15]. This is due to the fact that slight increase in threshold voltage causes a large amount of leakage power reduction with only small penalty in propagation delay. It is observed that increasing the threshold voltage between 0.2 V_{DD} and 0.4 V_{DD} gives the highest reduction in power with a minimal penalty in delay. Thereafter, the propagation delay increases quickly as V_{th} is increased beyond 0.4 V_{DD} and a high penalty in terms of speed has to be paid [4]. It is necessary to mention here that there is another incentive in not allowing the threshold voltage to increase beyond 0.4 V_{DD} which is that the threshold voltage value should be less than the switching threshold V_M= (0.5V_{DD}). If the threshold voltage is assigned a value that is higher than 0.4 V_{DD}, then due to any process variation the threshold voltage may reach V_M. Further equation (12) shows that increase in threshold voltage decreases subthreshold leakage current, so if threshold voltage is increased between 0.2 V_{DD} to 0.4 V_{DD} we can achieve low subthreshold leakage power for buffers and this behavior can lead to a significant reduction in total power dissipation with minimal increase in the propagation delay. In addition, the propagation delay penalty can be compensated by a slight increase in the number of buffer stages. Thus, an overall saving in both power dissipation and propagation delay can be achieved. The expression that gives the optimum threshold voltage which minimizes power delay square product as a function of the number of stages N , C_L/C_i ratio, and the weighing factors (a=1 and b=2), can be approximated by[5]and is given by

$$V_{thn} = \left(0.35 - 0.07\,\frac{N - N_{opt} - 1}{N_D - N_{opt}}\right)\left(1 + \ln\left(\frac{b}{2a}\right)\right) \quad (13)$$

Where N_D and N_{opt} are expressed in equation (3) and (4).

5. RESULTS AND DISCUSSIONS

Computations have been made analytically for parameters like number of stages, taper factor etc. under different load conditions and then SPICE simulation in 70 nm technology node is performed for conventional CMOS tapered buffer as well as for proposed taper buffer designs. Both the designs are compared and contrasted for performance metrics such as power dissipation and propagation delay.

For the buffer designed for first condition by selecting number of stages $N=N_D$ which reduces propagation delay irrespective of power dissipation, the results are summarized in table 1.Which shows an increase in propagation delay of around 2% and decrease in power dissipation of around 8% in the proposed design as compared to conventional design. This is because of the presence of feedback network which, uses more number of transistors as compared to conventional design, causes a small increase in propagation delay. Moreover the design is for minimum delay operation, hence the decrease in total power dissipation is also small. The results in Table 2 compares propagation delay and power dissipation for the proposed and conventional buffers designs for minimising power delay cost function by using number of *stages* $N=N_{opt}$. Comparison shows that power dissipation reduction in this case is more which is about 12% at the cost of increase in delay of about 4-5% and is due to the fact that number of stages $N=N_{opt,}$ (designed for minimising power delay cost function) are less than N_D. Beside this for C_L=15fF there is no change in power and delay because reduction in short circuit power using proposed design works for two or more than two stages. Finally table 3 tabulates the results for low power delay optimized buffer, which is achieved by making V_{th} as another variable during design. The results indicate that by increasing V_{th} to an optimum value between 0.2 volt to 0.4 volt not only decreases the leakage power and short circuit power for proposed buffer but the increase in propagation delay is also very small and can be mitigated by increasing the number of buffer stages. Table 3 shows an improvement in power dissipation of 14% to 15% at the same propagation delay which is achieved by using number of stages $N=N_{opt}+2$ for proposed buffer as compared to $N=N_{opt}+1$ for conventional buffer.

5. CONCLUSION

In this paper, power dissipation and propagation delay parameters have been optimized during design of CMOS buffer driving large capacitive loads. The short circuit power and subthreshold leakage power have been minimized to reduce total power dissipation in deep submicron (DSM) region. The proposed buffer has been designed in 70 nm technology node and simulated in SPICE environment. An improvement of 15% in power dissipation has been achieved while maintaining same delay as compared to the existing design. Hence, the proposed buffer can be used to provide power efficient solutions for portable VLSI applications at optimum propagation delay.

Table 1. Propagation delay and power dissipation for buffer stages $N=N_D$ (for minimum delay)

C_L (fF)	N_D	F_D	Tapper Buffer		Proposed Buffer		% increase in propagation delay	% decrease in power dissipation
			Propagation delay (ns)	Power dissipation (µW)	Propagation delay (ns)	Power dissipation (µW)		
15	2	3.16	0.0743	0.438	0.07673	0.39658	3.27	9.46
150	4	3.16	0.088	2.676	0.088924	2.41516	1.05	9.75
1500	5	3.98	0.0921	15.18	0.094123	13.8148	2.19	8.99
15000	7	3.72	0.08966	155.798	0.09153	141.7791	2.09	8.99
150000	9	3.59	0.0883	1600.67	0.090859	1472.925	2.89	7.98

Table 2. Propagation delay and power dissipation for buffer stages $N=N_{opt}$ (for minimising power delay cost function)

C_L (fF)	N_{opt}	F_{opt}	Tapper Buffer		Proposed Buffer		% increase in propagation delay	% decrease in power dissipation
			Propagation delay (ns)	Power dissipation (µW)	Propagation delay (ns)	Power dissipation (µW)		
15	1	3.16	0.1329	0.1825	0.1329	0.1825	0	0
150	2	4.64	0.1246	1.051	0.128339	0.91018	3.01	13.39
1500	3	5.62	0.1296	5.597	0.134851	4.93516	4.05	11.82
15000	4	6.31	0.1239	55.156	0.128919	48.5333	4.05	12.00
150000	5	6.81	0.1251	533.521	0.130994	469.5985	4.71	11.98

Table 3. Propagation delay and power dissipation for buffer stages $N=N_{opt}+1$and $N=N_{opt}+2$ with variable V_{th}

C_L (fF)	V_{thn}	Tapper Buffer			Proposed Buffer			% increase in propagation delay	% decrease in power dissipation
		N_{opt+1}	Propagation delay (ns)	Power dissipation (µW)	N_{opt+2}	Propagation delay (ns)	Power dissipation (µW)		
15	0.35	2	0.11131	0.0467	3	0.113169	0.04042	1.67	13.45
150	0.35	3	0.12191	0.5158	4	0.121659	0.43804	-0.25	15.08
1500	0.35	4	0.12296	1.879	5	0.12317	1.61173	0.171	14.23
15000	0.36	5	0.12521	25.55	6	0.126028	22.1085	0.659	13.47
150000	0.35	6	0.12599	205.23	7	0.127224	175.3101	0.960	14.58

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