Abstract

As technology scales down, timing verification of digital integrated circuits becomes an extremely difficult task due to statistical variations in the gate and wire delays. Statistical timing analysis techniques are being developed to tackle this problem. The variations of critical dimensions in modern VLSI technologies lead to variability in interconnect performance that must be fully accounted for the timing verification. However, handling a multitude of inter-die/intra-die variations and assessing their impacts on circuit performances can dramatically complicate the timing analysis. For optimizations like physical synthesis and static timing analysis, efficient interconnect delay and slew computation is critical. Slew indicates the rate of change of input/output signals. Slew rate determines the ability of a device to handle the varying signals. Determination of slew rate to a good proximity is thus very much essential for efficient design of high speed CMOS integrated circuits as the increase in waveform slew directly enhances the delay of the interconnections. This work presents an accurate and efficient model to compute the slew metric of on-chip interconnect of high speed CMOS circuits.
Our slew metric assumption is based on the Gamma Distribution Function. The gamma distribution is used to characterize the normalized homogeneous portion of the step response. For a generalized RC interconnect model, the stability of the Gamma Distribution model is guaranteed. The better accuracy is proved by comparing our approach with the established methods and SPICE results. It is shown that our approach could result in the error in slew calculation as low as 2% with lower value of driver resistance when compared with the SPICE results.

Reference


Index Terms

Electronics Integrated Circuits
### Key words

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