A Novel and Efficient Approach for RC Delay Evaluation of On-chip VLSI Interconnect under Current Mode Signaling Technique

Abstract

Current-mode signaling significantly increases the bandwidth of on-chip interconnects compared to voltage mode signaling and reduces the overall propagation delay. A delay formula for current mode is necessary for estimation of delay and bandwidth for VLSI systems. In this paper, closed-form expression of delay model based on the effective lumped element resistance and capacitance approximation of distributed RC lines are presented. A new closed-form solution of delay under step input excitation is developed. The usefulness of this solution is that both resistive and capacitive load termination is accurately modeled for use in current mode signaling. Comparison of simulation results with other established models justifies the accuracy of our approach.

Reference

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Index Terms

Electronics VLSI

Key words

Current mode signaling On-chip Interconnect

Moment matching

MNA Analysis

Delay Calculation