Abstract

REDEFINE [3] is a polymorphic ASIC, in which arbitrary computational structures on hardware are defined at runtime. The REDEFINE execution fabric comprises Compute Elements (CEs) interconnected by a Honeycomb network, which also serves as the distributed Network-on-chip. Each computational structure is dynamically assigned to a subset of the CEs on the execution fabric by the REDEFINE support logic. A HLL specification of the application is compiled into Hyper Operations (HyperOps) by the REDEFINE compiler [3], where each HyperOp is a set of interacting operations. The compiler also determines partitions of the HyperOps (pHyperOps) that can be assigned to CEs to suitably meet the structural constraints of the execution fabric. In this paper we propose an algorithm to map HyperOps onto Computational Structures. A pHyperOp communication graph (PCG) captures the communication between the various pHyperOps. Through a sequence of transformations, the
PCG is transformed into a Cayley tree. The Cayley tree is then overlayed on the Cayley graph to form a computational structure. The proposed mapping algorithm offers a solution that incurs a penalty 18% on average over that of the optimal.

Reference


Index Terms

Computer Science  Graphics
### Key words

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