Abstract

In microelectronics design, power consumption, speed of operation, are crucial constraints. Propagation delay of circuit component has an impact on such factors. Pipelining and parallel processing strategies are utilized for desirable propagation delays and hence for clock and throughput variation respectively. To some extent variation in propagation delay is responsible for power consumption reduction. In this paper, pipelining and parallel processing concepts are analyzed with reference to task scheduling in real time system. Power consumption and speed of operation issues of such systems are analyzed.

Reference

[8] Ramesh Mishra, Namrata Rastogi, Dakai Zhu, “Energy aware scheduling for distributed real time systems,” in proc. of Int. symposium on Parallel and Distributed Processing, IPDP-03, Nice, France.

**Index Terms**

Electronics

Microelectronics Design

**Key words**

VLSI

power consumption

critical path

DVS

DFS