In this paper an effective hardware design methodology for the devices like mobile phones, digital cameras, etc is described. In those devices only few applications are running at given time. So it requires only few hardware blocks to be active. This design approach is based on the idea of configuring and programming the hardware of active application whenever required at a single Field Programmable Gate Array (FPGA) chip.

It requires effective hardware-software controller to configured required hardware for active application. In case of multiple applications running in-parallel, it is
necessary to configure all the hardware required for these applications to be configured independently. To support this feature, the proposed design methodology introduces the concept of FPGA partitioning to configure these active parallel hardware designs where new designs can be configured at free un-configured partitions using partial configuration without disturbing the hardware of running application.

Using this approach single FPGA chip can be configured dynamically for active application(s) only instead of configuring hardware design for all active and in-active applications thereby reducing the overall hardware, cost, size, power consumption and enhancing battery life.

This paper explains about redesigning FPGA architecture to introduce FPGA Partitions, Partial & fast programming and Hardware-Software co-design methodology suitable for the devices which are running applications in parallel.

Reference

- www.actel.com for Actel FPGA architecture and programming
- www.xilinx.com for Xilinx FPGA architecture

Index Terms

Electronics Hardware Design

Key words

Parallel applications

Dynamic Partial Reconfiguration

FPGA Partitions
Hardware-software co-design for various Parallel applications using the Concept of Dynamic Partial Reconfiguration at FPGA Partitions