Abstract

This paper presents a novel pseudo 4 phase dual rail protocol with self reset logic suited for high speed asynchronous applications. The traditional 4 phase dual rail requires the input to be of alternating valid and empty cycles. However the proposed pseudo 4 phase involves continuous stream of valid data without a separate empty cycle. The empty phase is generated internally so that the next valid data can be processed. Also self reset logic for dual rail protocol has been proposed in which the combinational blocks resets itself whenever its evaluation phase is completed and the data is latched at the pipeline register. The concept of multiple reset i.e. resetting each of the gates in the combinational block between any two pipeline registers simultaneously has been introduced reducing the reset phase and hence increasing the throughput rate. An asynchronous 8 bit pipelined carry propagate adder was implemented in .18 um technology. The reset phase has reduced by 63.25% and 47.63%
compared to the design without self and multiple reset for logic depth of three and two respectively. The results show that the reset phase varies inversely with the logic depth for the proposed design.

**Reference**


**Index Terms**

Electronics Communication Systems

**Key words**

pseudo 4 phase

self reset

multiple reset

dual rail

asynchronous