Abstract

This paper explores the design approach of a low power high performance Multiply and Accumulate (MAC) unit with hybrid encoded Reduced Transition Activity Technique (RTAT) equipped multiplier and low power 0.13µm adder. Design of a low power MAC unit for image processing systems exploiting insignificant bits in pixels values and the similarity of neighboring pixels in video streams is presented in this paper. The proposed technique reduces dynamic power consumption by analyzing the bit patterns in the input data to reduce switching activities. Special values of the pixels in the video streams such as zero, one, repeated values or repeated bit combinations are detected and data paths in the architecture design are disabled appropriately to eliminate unnecessary switching in arithmetic units. The hybrid encoder in the low power multiplier uses both the Booth and proposed technique. If the number of 1's less than or equal to three the proposed encoding technique used otherwise go for Booth technique. By this proposed technique the number of partial products reduced by this reduction in switching activity also. The proposed adder cell used in the MAC block consumes less power than the other previous adder techniques. This high performance low power MAC can be used in image processing. It is observed from the device level simulation using TANNER 12.6 EDA that the proposed scheme helps to reduce operations and switching activities in the MAC unit up to 19% and saves power up to 46%.
Modified Multiply and Accumulate Unit with Hybrid Encoded Reduced Transition Activity Technique Equipped Multiplier and Low Power 0.13µm Adder for Image Processing Applications

Reference

- M. Vesterbacka, “A 14-transistor CMOS full adder with full voltage swing nodes,” in Proc.

Index Terms

Electronics
Performance Analysis and Design Aids

Key words
Low power
Booth Multiplier

MAC

RTAT