This paper proposes multilevel inverter type DSTATCOM for mitigating voltage sag at the load side. Cascaded H-bridge configuration for multilevel inverter with advanced phase shifted pulse width modulation technique is presented. Voltage sags are generated by faults the distribution feeder. First addresses with the three-phase 5-level cascaded multi level inverter and second addresses with the three-phase 7-level cascaded multi level inverter based on the shunt active power filter for mitigating the voltage disturbances. The proposed multilevel topology is simulated using MATLAB. The simulation results of the Five-level and Seven-level cascaded multilevel inverters are compared in different aspects.

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**Index Terms**

Computer Science Power Systems

**Key words**

MLCI (Multilevel Cascaded Inverter) DSTATCOM Distribution

static compensator

(VSC) Voltage Source Converter

THD (Total Harmonic Distortion) mitigation